



RV-8063-C8

Development Board

:: Micro Crystal AG Muehlestrasse 14 CH-2540 Grenchen Switzerland

Internet www.microcrystal.com Email sales@microcrystal.com



Development Board

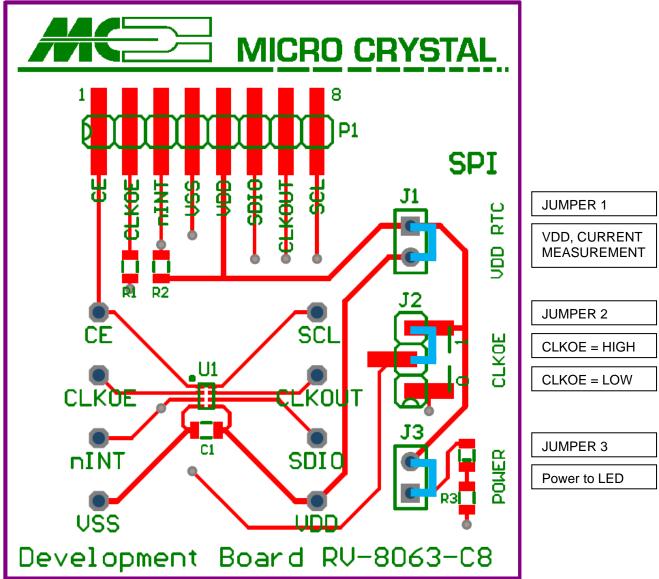
RV-8063-C8

The RV-8063-C8 is soldered (U1) onto the Development Board. Every pin is either accessible at test pins 1 - 8 or at the test vias situated around the device.

The following passive components are already soldered on the Board:

C1	10 nF	Decoupling capacitor between VSS and VDD.
R1	10 kΩ	Protection resistor to prevent short-circuit between external CLKOE signal and Jumper.
R2	10 kΩ	Pull-up resistor INT to VDD.
R3 LED	330 Ω green	Current limiting resistor for LED. Supply on, current consumption of the LED must be considered.

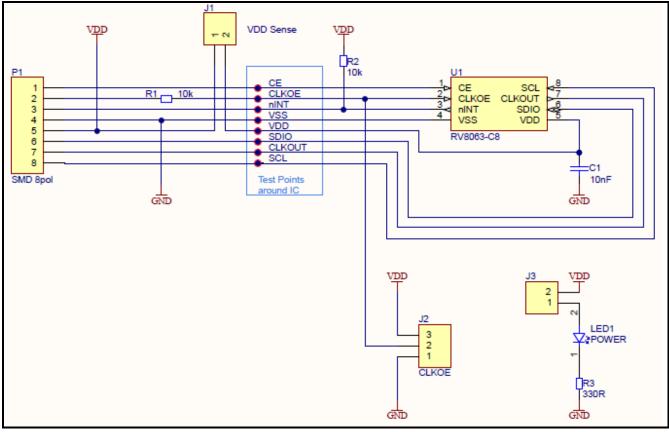
DEVELOPMENT BOARD



Development Board

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SCHEMATICS



PINOUT RV-8063-C8

#8 #5		
	# 1 CE	# 8 SCL
	# 2 CLKOE	# 7 CLKOUT
	# 3 INT	# 6 SDIO
#1 #4	# 4 Vss	# 5 V _{DD}

PIN DESCRIPTION

Symbol	Pin #	Description
CE	1	Chip Enable Input; when LOW, the interface is reset; may not be wired permanently HIGH.
CLKOE	2	Input to enable the CLKOUT pin. If CLKOE is HIGH, the CLKOUT pin is in output mode. When CLKOE is tied to Ground, the CLKOUT pin is LOW.
INT	3	Interrupt Output; open-drain; active LOW; requires pull-up resistor; Used to output alarm, minute, half minute, countdown timer and compensation Interrupt signals.
V _{SS}	4	Ground.
V _{DD}	5	Power Supply Voltage
SDIO	6	Serial Data Input and Output. Input: When CE is LOW, input may float. Output: Push-pull output; drives from Vss to Vbb; is high-impedance when not driving.
CLKOUT	7	Clock Output; push-pull; controlled by CLKOE. If CLKOE is HIGH (VDD), the CLKOUT pin drives the square wave of 32.768 kHz, 16.384 kHz, 8.192 kHz, 4.096 kHz, 2.048 kHz, 1.024 kHz or 1 Hz (Default value is 32.768 kHz). When CLKOE is tied to Ground, the CLKOUT pin is LOW.
SCL	8	Serial Clock Input. When CE is LOW, this input may float.

Datasheet and Application-Manual are available for download under: https://www.microcrystal.com