# Application Manual

# RV-8564-C3

## Real-Time Clock Module with I²C-Bus Interface

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# RV-8564-C3

## Real-Time Clock Module with I²C-Bus Interface

## 1. OVERVIEW

- RTC module with built-in “Tuning Fork” crystal oscillating at 32.768 kHz
- Counters for seconds, minutes, hours, date, month, year, century and weekday
- Automatic leap year calculation (2000 to 2099)
- Century bit
- Alarm Interrupts for date, weekday, hour and minute settings
- Periodic Countdown Timer Interrupt function
- Internal Power-On Reset (POR)
- Low voltage detector
- Programmable Clock Output for peripheral devices (32.768 kHz, 1024 Hz, 32 Hz, 1 Hz)
- I²C-bus interface (up to 400 kHz)
- Wide Timekeeping voltage range: 1.2 V to 5.5 V
- Wide interface operating voltage: 1.8 to 5.5 V
- Low power consumption: 250 nA ($V_{DD}$ = 3.0 V, $T_A$ = 25°C)
- Operating temperature range: -40 to +85°C
- Small and compact C3 package size (3.7 x 2.5 x 0.9 mm), RoHS-compliant and 100% lead-free
- Automotive qualification according to AEC-Q200 available

### 1.1. GENERAL DESCRIPTION

The RV-8564-C3 is a CMOS real-time clock / calendar optimized for low power consumption. A programmable clock output, interrupt output and voltage low detector are also provided. All addresses and data are transferred over an I²C-bus interface for communication with a host controller. The Address Pointer is incremented automatically after each written or read data byte.

## 1.2. APPLICATIONS

The RV-8564-C3 RTC module combines standard RTC functions in high reliable, small ceramic package:

- Small RTC module (embedded XTAL) in a small 3.7 x 2.5 x 0.9 mm lead-free ceramic package
- Price competitive

The small size and the competitive pricing make this product perfectly suitable for many applications:

- Communication: IoT / Wearables / Wireless Sensors and Tags / Handsets
- Automotive: M2M / Navigation & Tracking Systems / Dashboard / Tachometers / Engine Controller Car Audio & Entertainment Systems
- Metering: E-Meter / Heating Counter / Smart Meters / PV Converter
- Outdoor: ATM & POS systems / Surveillance & Safety systems / Ticketing Systems
- Medical: Glucose Meter / Health Monitoring Systems
- Safety: Security & Camera Systems / Door Lock & Access Control
- Consumer: Gambling Machines / TV & Set Top Boxes / White Goods
- Automation: PLC / Data Logger / Home & Factory Automation / Industrial and Consumer Electronics

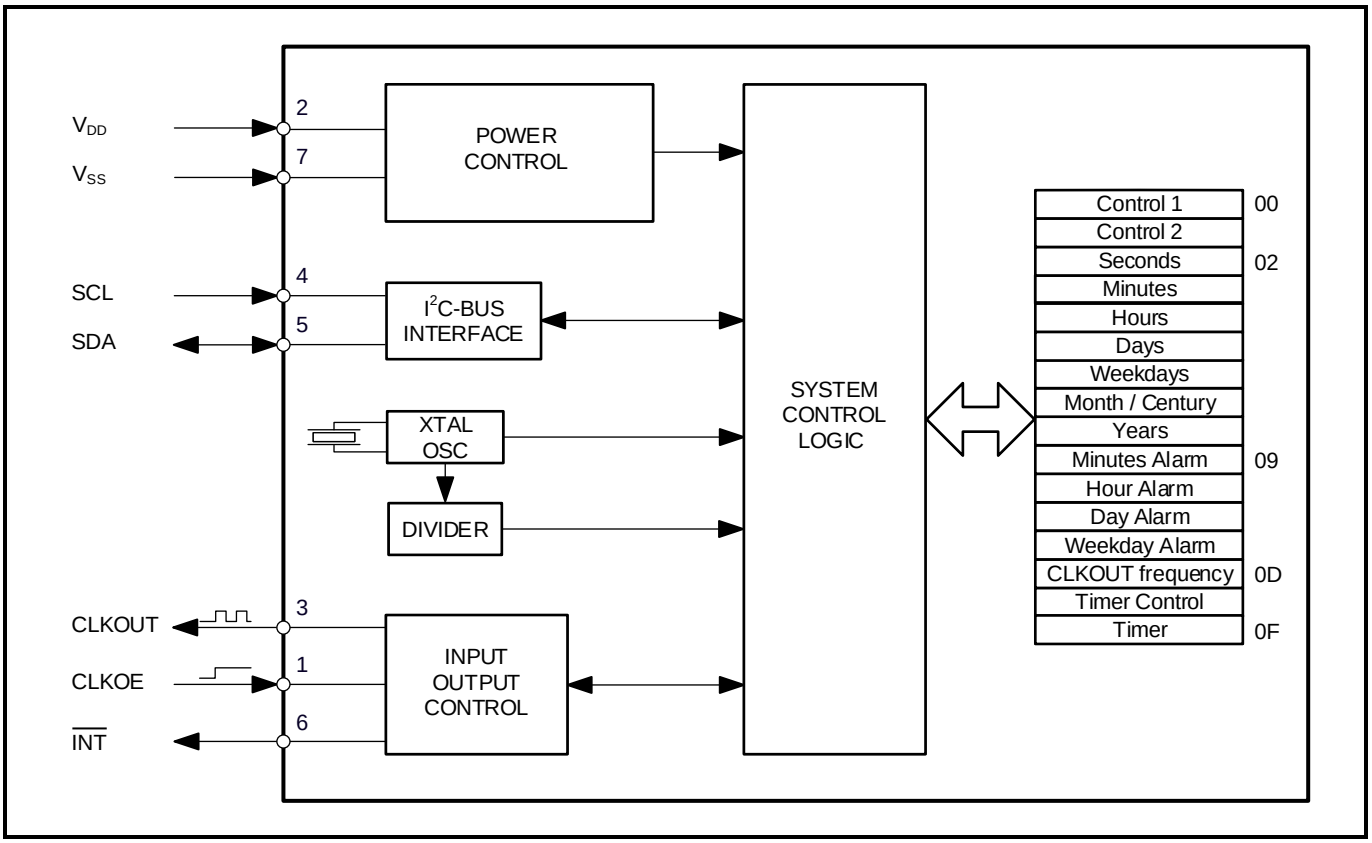
## 1.3. ORDERING INFORMATION

Example: RV-8564-C3 TA QC

| Code | Operating temperature range |
|---|---|
| TA (Standard) | -40 to +85°C |

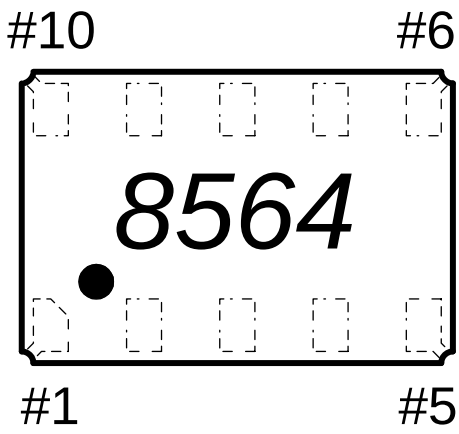
| Code | Qualification |
|---|---|
| QC (Standard) | Commercial Grade |
| QA | Automotive Grade AEC-Q200 |

## 2. BLOCK DIAGRAM



## 2.1. PINOUT

**RV-8564-C3 Package: (top view)**




| | |
|---|---|
| #1 | CLKOE |
| #2 | $V_{DD}$ |
| #3 | CLKOUT |
| #4 | SCL |
| #5 | SDA |
| #6 | $\overline{INT}$ |
| #7 | $V_{SS}$ |
| #8 | NC |
| #9 | NC |
| #10 | NC |

## 2.2. PIN DESCRIPTION

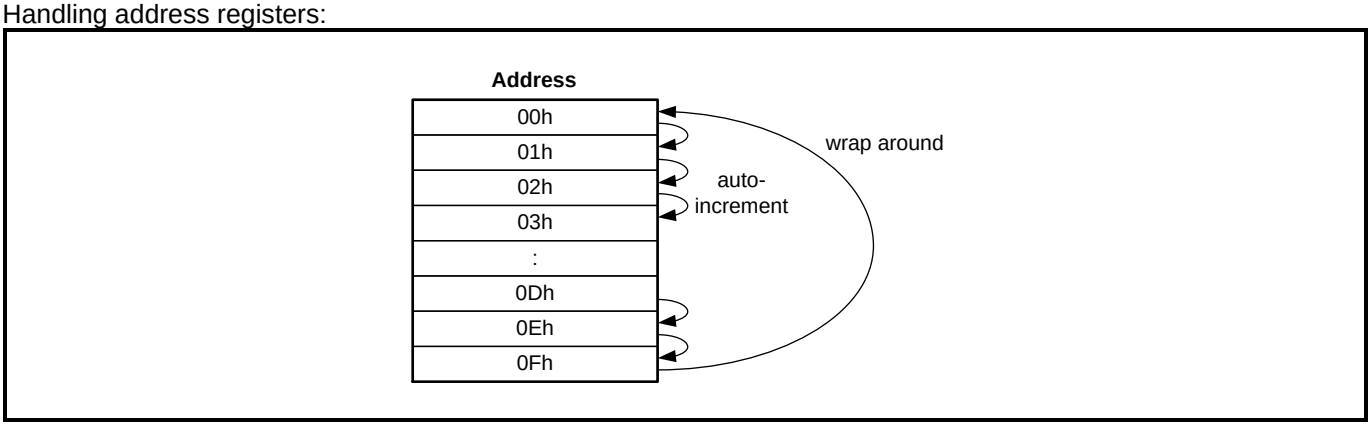
| Symbol | Pin # | Description |
|---|---|---|
| CLKOE | 1 | Input to enable the CLKOUT pin. If CLKOE is HIGH, the CLKOUT pin is in output mode. When CLKOE is tied to Ground, the CLKOUT pin is LOW. |
| $V_{DD}$ | 2 | Power Supply Voltage. |
| CLKOUT | 3 | Clock Output; push-pull; controlled by CLKOE. If CLKOE is HIGH ($V_{DD}$), the CLKOUT pin drives the square wave of 32.768 kHz, 1024 Hz, 32 Hz or 1 Hz (Default value is 32.768 kHz). When CLKOE is tied to Ground, the CLKOUT pin is LOW. |
| SCL | 4 | I²C Serial Clock Input; requires pull-up resistor. |
| SDA | 5 | I²C Serial Data Input-Output; open-drain; requires pull-up resistor. |
| $\overline{INT}$ | 6 | Interrupt Output; open-drain; active LOW; requires pull-up resistor. Used to output Alarm and Periodic Countdown Timer Interrupt signals. |
| $V_{SS}$ | 7 | Ground. |
| NC | 8 | Not connected. |
| NC | 9 | Not connected. |
| NC | 10 | Not connected. |

## 2.3. FUNCTIONAL DESCRIPTION

The RV-8564-C3 is a low power CMOS real-time clock/calendar module with embedded 32.768 kHz Crystal. The CMOS IC contains 16 8-bit registers with an auto-incrementing register address, a frequency divider which provides the source clock for the Real Time Clock (RTC), a programmable clock output, a timer, a voltage low detector, and a 400 kHz I²C-bus interface.

The built-in address register will increment automatically after each read or write of a data byte up to the register 0Fh. After register 0Fh, the auto-incrementing will wrap around to address 00h (see following Figure).

Handling address registers:



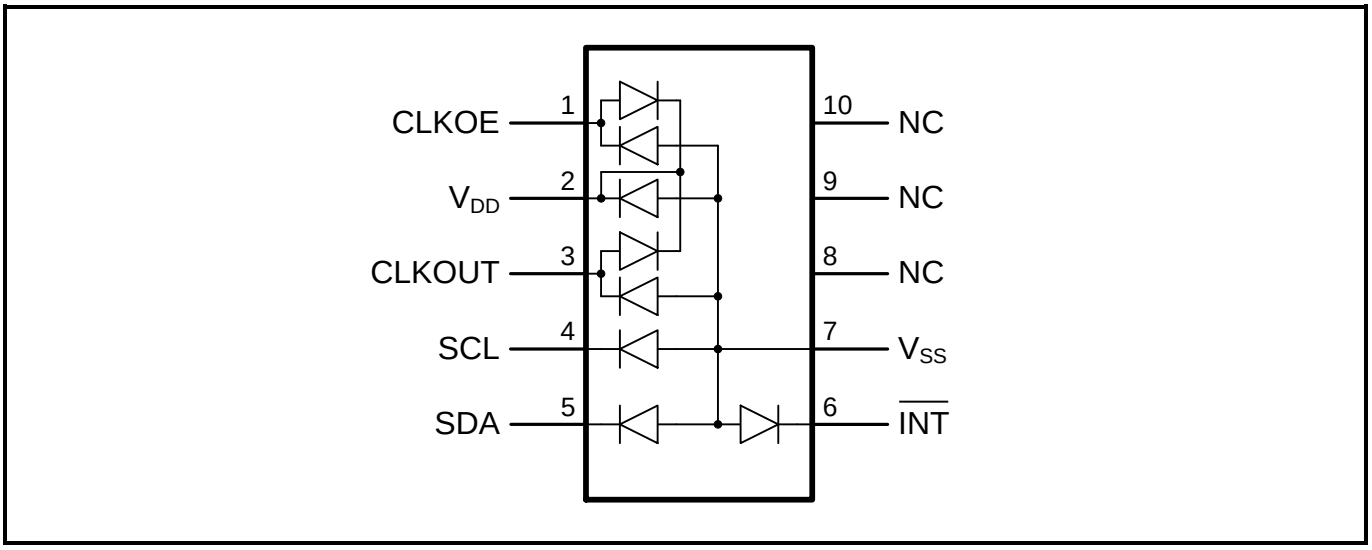

All registers (see REGISTER OVERVIEW) are designed as addressable 8-bit parallel registers although not all bits are implemented.

- The first two registers (memory address 00h and 01h) are used as control and status register.
- The addresses 02h through 08h are used as counters for the clock function (seconds up to years counters).
- Address locations 09h through 0Ch contain alarm registers which define the conditions for an alarm.
- Address 0Dh controls the CLKOUT output frequency
- The registers at 0Eh and 0Fh are for the timer function.

The Seconds, Minutes, Hours in 24-hour format, Days, Weekdays, Months, and Years, as well as the corresponding alarm registers are all coded in Binary Coded Decimal (BCD) format.

When one of the RTC registers is written or read, the contents of all time counters (memory locations 02h through 08h) are frozen. Therefore, faulty writing or reading of the clock and calendar during a carry condition is prevented for up to 1 second. The pending 1 Hz tick is correctly applied.

## 2.4. DEVICE PROTECTION DIAGRAM



# 3. REGISTER ORGANIZATION

Registers are accessed by selecting a register address and then performing read or write operations. Multiple reads or writes may be executed in a single access, with the address automatically incrementing after each byte.
16 registers (00h – 0Fh) are available. The time registers are encoded in the Binary Coded Decimal format (BCD) to simplify application use. Other registers are either bit-wise or standard binary format. When one of the RTC registers is written or read, the contents of all time counters are frozen for up to 1 second and the pending 1 Hz tick is correctly applied. Therefore, faulty writing or reading of the clock and calendar during a carry condition is prevented.

## 3.1. REGISTER OVERVIEW

After reset, all registers are set according to Table in section REGISTER RESET VALUES SUMMARY.

| Address | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 00h | Control1 | TEST1 | N | STOP | N | TESTC | N | N | N |
| 01h | Control2 | N | N | N | TI_TP | AF | TF | AIE | TIE |
| 02h | Seconds | VL | 40 | 20 | 10 | 8 | 4 | 2 | 1 |
| 03h | Minutes | X | 40 | 20 | 10 | 8 | 4 | 2 | 1 |
| 04h | Hours | X | X | 20 | 10 | 8 | 4 | 2 | 1 |
| 05h | Date | X | X | 20 | 10 | 8 | 4 | 2 | 1 |
| 06h | Weekdays | X | X | X | X | X | 4 | 2 | 1 |
| 07h | Months / Century | CB | X | X | 10 | 8 | 4 | 2 | 1 |
| 08h | Years | 80 | 40 | 20 | 10 | 8 | 4 | 2 | 1 |
| 09h | Minutes Alarm | AE_M | 40 | 20 | 10 | 8 | 4 | 2 | 1 |
| 0Ah | Hours Alarm | AE_H | X | 20 | 10 | 8 | 4 | 2 | 1 |
| 0Bh | Date Alarm | AE_D | X | 20 | 10 | 8 | 4 | 2 | 1 |
| 0Ch | Weekday Alarm | AE_W | X | X | X | X | 4 | 2 | 1 |
| 0Dh | CLKOUT Frequency | FE | X | X | X | X | X | FD | |
| 0Eh | Timer Control | TE | X | X | X | X | X | TD | |
| 0Fh | Timer Value | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 |

Bit positions labeled as X are not implemented.
The bit position labeled with N should always be written with logic 0.

## 3.2. CONTROL REGISTERS

### 00h - Control1

Control and status register 1.

| Address | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 00h | Control1 | TEST1 | N | STOP | N | TESTC | N | N | N |
| | Reset | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| | Set TESTC to 0 | | | | | 0 | | | |

| Bit | Symbol | Value | Description |
|---|---|---|---|
| 7 | TEST1 | 0 | Normal mode. |
| | | 1 | External clock test mode. Do not use. |
| 6 | N | 0 | Should always be written with logic 0. |
| 5 | STOP | | STOP bit (see STOP BIT FUNCTION) |
| | | 0 | RTC clock runs. |
| | | 1 | RTC divider chain flip-flops are asynchronously set to logic 0.<br>The RTC clock is stopped (CLKOUT at 32.768 kHz is still available). |
| 4 | N | 0 | Should always be written with logic 0. |
| 3 | TESTC | 0 | Must be set to logic 0 for normal operations. |
| | | 1 | Test mode. – Default value |
| 2:0 | N | 0 | Should always be written with logic 0. |

Note that the two bits TEST1 and TESTC are for device testing. Make sure TEST1 and TESTC are set to 0 during normal operation. If accidentally set to 1, they may modify the clock data or result in abnormal time.

### 01h – Control2

Control and status register 2.

| Address | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 01h | Control2 | N | N | N | TI_TP | AF | TF | AIE | TIE |
| | Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Set N (Bit 7) to 0 | 0 | | | | | | | |

| Bit | Symbol | Value | Description |
|---|---|---|---|
| 7:5 | N | 000 | Should always be written with logic 0. |
| 4 | TI_TP | | Periodic Countdown Timer Interrupt Mode.<br>How the setting of TI_TP and the Periodic Countdown Timer Flag TF can affect the $\overline{INT}$ pulse generation is explained in sections PERIODIC COUNTDOWN TIMER INTERRUPT FUNCTION. |
| | | 0 | Interval Mode. Interrupt follows Periodic Countdown Timer Flag TF.<br>– Default value |
| | | 1 | Pulse Mode. Interrupt generates a pulse. |
| 3 | AF | | Alarm Flag (see ALARM FUNCTION and INTERRUPT OUTPUT) |
| | | 0 | Alarm Flag inactive. |
| | | 1 | Alarm Flag active. Can be cleared by writing a 0 to the bit. |
| 2 | TF | | Periodic Countdown Timer Flag (see PERIODIC COUNTDOWN TIMER INTERRUPT FUNCTION, INTERRUPT OUTPUT and PERIODIC COUNTDOWN TIMER FLAG TF) |
| | | 0 | No Countdown Timer Interrupt generated. |
| | | 1 | Flag set when Periodic Countdown Timer Interrupt generated. |
| 1 | AIE | | Alarm Interrupt Enable (see ALARM FUNCTION and INTERRUPT OUTPUT) |
| | | 0 | Disabled |
| | | 1 | Enabled |
| 0 | TIE | | Periodic Countdown Timer Interrupt Enable (see INTERRUPT OUTPUT) |
| | | 0 | Disabled |
| | | 1 | Enabled |

## 3.3. TIME AND DATE REGISTERS

### 02h - Seconds

This register holds the count of seconds, in two binary coded decimal (BCD) digits. Values will be from 00 to 59.

| Address | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 02h | Seconds | VL | 40 | 20 | 10 | 8 | 4 | 2 | 1 |
| | Reset | 1 | X | X | X | X | X | X | X |

| Bit | Symbol | Value | Description |
|---|---|---|---|
| 7 | VL | | Voltage Low Flag (see VOLTAGE LOW FLAG) |
| | | 0 | Clock integrity is guaranteed. |
| | | 1 | Clock integrity is not guaranteed; oscillator has stopped or has been interrupted. – Default value |
| 6:0 | Seconds | 00 to 59 | Holds the count of seconds, coded in BCD format. |

### 03h - Minutes

This register holds the count of minutes, in two binary coded decimal (BCD) digits. Values will be from 00 to 59.

| Address | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 03h | Minutes | X | 40 | 20 | 10 | 8 | 4 | 2 | 1 |
| | Reset | X | X | X | X | X | X | X | X |

| Bit | Symbol | Value | Description |
|---|---|---|---|
| 7 | X | 0 or 1 | Unused |
| 6:0 | Minutes | 00 to 59 | Holds the count of minutes, coded in BCD format. |

### 04h - Hours

This register holds the count of hours, in two binary coded decimal (BCD) digits. Values will be from 00 to 23.

| Address | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 04h | Hours | X | X | 20 | 10 | 8 | 4 | 2 | 1 |
| | Reset | X | X | X | X | X | X | X | X |

| Bit | Symbol | Value | Description |
|---|---|---|---|
| 7:6 | X | 0 or 1 | Unused |
| 5:0 | Hours | 00 to 23 | Holds the count of hours, coded in BCD format. |

### 05h – Date

This register holds the current date of the month, in two binary coded decimal (BCD) digits. Values will range from 01 to 31. Leap years are correctly handled from 2000 to 2099.

| Address | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 05h | Date | X | X | 20 | 10 | 8 | 4 | 2 | 1 |
| | Reset | X | X | X | X | X | X | X | X |

| Bit | Symbol | Value | Description |
|---|---|---|---|
| 7:6 | X | 0 or 1 | Unused |
| 5:0 | Date | 01 to 31 | Holds the current date of the month, coded in BCD format. |

### 06h - Weekdays

This register holds the current day of the week. Each value represents one weekday that is assigned by the user. Values will range from 0 to 6.

| Address | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 06h | Weekdays | X | X | X | X | X | 4 | 2 | 1 |
| | Reset | X | X | X | X | X | X | X | X |

| Bit | Symbol | Value | Description |
|---|---|---|---|
| 7:3 | X | 0 or 1 | Unused |
| 2:0 | Weekdays | 0 to 6 | Holds the weekday counter value. |

| Weekdays | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| Weekday 1 | X | X | X | X | X | 0 | 0 | 0 |
| Weekday 2 | | | | | | 0 | 0 | 1 |
| Weekday 3 | | | | | | 0 | 1 | 0 |
| Weekday 4 | | | | | | 0 | 1 | 1 |
| Weekday 5 | | | | | | 1 | 0 | 0 |
| Weekday 6 | | | | | | 1 | 0 | 1 |
| Weekday 7 | | | | | | 1 | 1 | 0 |

### 07h – Months / Century

This register holds the Century Bit CB and the current month, in two binary coded decimal (BCD) digits. Values will range from 01 to 12.

| Address | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 07h | Months / Century | CB | X | X | 10 | 8 | 4 | 2 | 1 |
| | Reset | X | X | X | X | X | X | X | X |

| Bit | Symbol | Value | Description |
|---|---|---|---|
| 7 | CB | | Century Bit. This bit will be toggled when the Years register rolls over from 99 to 00. This bit may be re-assigned by the user. The user can define the meaning of CB (1 for current century and 0 for next century, or 0 for current century and 1 for next century). |
| | | 0 | Toggles from 0 to 1 if Years register rolls over from 99 to 00. |
| | | 1 | Toggles from 1 to 0 if Years register rolls over from 99 to 00. |
| 6:5 | X | 0 or 1 | Unused |
| 4:0 | Months / Century | 01 to 12 | Holds the current month, coded in BCD format. |

| Months | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| January | CB | X | X | 0 | 0 | 0 | 0 | 1 |
| February | | | | 0 | 0 | 0 | 1 | 0 |
| March | | | | 0 | 0 | 0 | 1 | 1 |
| April | | | | 0 | 0 | 1 | 0 | 0 |
| May | | | | 0 | 0 | 1 | 0 | 1 |
| June | | | | 0 | 0 | 1 | 1 | 0 |
| July | | | | 0 | 0 | 1 | 1 | 1 |
| August | | | | 0 | 1 | 0 | 0 | 0 |
| September | | | | 0 | 1 | 0 | 0 | 1 |
| October | | | | 1 | 0 | 0 | 0 | 0 |
| November | | | | 1 | 0 | 0 | 0 | 1 |
| December | | | | 1 | 0 | 0 | 1 | 0 |

### 08h - Years

This register holds the current year, in two binary coded decimal (BCD) digits. Values will range from 00 to 99. Leap years are correctly handled from 2000 to 2099.

| Address | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 08h | Years | 80 | 40 | 20 | 10 | 8 | 4 | 2 | 1 |
| | Reset | X | X | X | X | X | X | X | X |

| Bit | Symbol | Value | Description |
|---|---|---|---|
| 7:0 | Years | 00 to 99 | Holds the current year, coded in BCD format. |

## 3.4. ALARM REGISTERS

### 09h – Minutes Alarm

This register holds the Minutes Alarm Enable bit AE_M and the alarm value for minutes, in two binary coded decimal (BCD) digits. Values will range from 00 to 59.

| Address | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 09h | Minutes Alarm | AE_M | 40 | 20 | 10 | 8 | 4 | 2 | 1 |
| | Reset | 1 | X | X | X | X | X | X | X |

| Bit | Symbol | Value | Description |
|---|---|---|---|
| 7 | AE_M | | Minutes Alarm Enable bit (see ALARM FUNCTION) |
| | | 0 | Enabled |
| | | 1 | Disabled – Default value |
| 6:0 | Minutes Alarm | 00 to 59 | Holds the alarm value for minutes, coded in BCD format. |

### 0Ah - Hours Alarm

This register holds the Hours Alarm Enable bit AE_H and the alarm value for hours, in two binary coded decimal (BCD) digits. Values will range from 00 to 23.

| Address | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0Ah | Hours Alarm | AE_H | X | 20 | 10 | 8 | 4 | 2 | 1 |
| | Reset | 1 | X | X | X | X | X | X | X |

| Bit | Symbol | Value | Description |
|---|---|---|---|
| 7 | AE_H | | Hours Alarm Enable bit (see ALARM FUNCTION) |
| | | 0 | Enabled |
| | | 1 | Disabled – Default value |
| 6 | X | 0 or 1 | Unused |
| 5:0 | Hours Alarm | 00 to 23 | Holds the alarm value for hours, coded in BCD format. |

### 0Bh - Date Alarm

This register holds the Date Alarm Enable bit AE_D and the alarm value for the date, in two binary coded decimal (BCD) digits. Values will range from 01 to 31.

| Address | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0Bh | Date Alarm | AE_D | X | 20 | 10 | 8 | 4 | 2 | 1 |
| | Reset | 1 | X | X | X | X | X | X | X |

| Bit | Symbol | Value | Description |
|---|---|---|---|
| 7 | AE_D | | Date Alarm Enable bit (see ALARM FUNCTION) |
| | | 0 | Enabled |
| | | 1 | Disabled – Default value |
| 6 | X | 0 or 1 | Unused |
| 5:0 | Date Alarm | 01 to 31 | Holds the alarm value for the date, coded in BCD format. |

### 0Ch – Weekday Alarm

This register holds the Weekday Alarm Enable bit AE_W and the alarm value for the weekday, in two binary coded decimal (BCD) digits. Values will range from 0 to 6.

| Address | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0Ch | Weekday Alarm | AE_W | X | X | X | X | 4 | 2 | 1 |
| | Reset | 1 | X | X | X | X | X | X | X |

| Bit | Symbol | Value | Description |
|---|---|---|---|
| 7 | AE_W | | Weekday Alarm Enable bit (see ALARM FUNCTION) |
| | | 0 | Enabled |
| | | 1 | Disabled – Default value |
| 6:3 | X | 0 or 1 | Unused |
| 2:0 | Weekday Alarm | 0 to 6 | Holds the weekday alarm value, coded in BCD format. |

## 3.5. CLKOUT REGISTER

### 0Dh – CLKOUT Frequency

A programmable square wave output is available at CLKOUT pin. Operation is controlled by the FE bit in register CLKOUT Frequency, and the Clock Output Enable pin (CLKOE) (see CLKOUT FREQUENCY SELECTION).

| Address | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0Dh | CLKOUT Frequency | FE | X | X | X | X | X | FD | |
| | Reset | 1 | X | X | X | X | X | 0 | 0 |

| Bit | Symbol | Value | Description |
|---|---|---|---|
| 7 | FE | | CLKOUT Enable bit (see CLKOUT FREQUENCY SELECTION) |
| | | 0 | The CLKOUT output is inhibited and set to logic 0. |
| | | 1 | The CLKOUT output is activated. – Default value |
| 6:2 | X | 0 or 1 | Unused |
| 1:0 | FD | | CLKOUT Frequency selection (see CLKOUT FREQUENCY SELECTION) |
| | | 00 | 32.768 kHz – Default value |
| | | 01 | 1024 Hz |
| | | 10 | 32 Hz |
| | | 11 | 1 Hz |

## 3.6. PERIODIC COUNTDOWN TIMER CONTROL REGISTERS

### 0Eh – Timer Control

This register controls the Periodic Countdown Timer function.

| Address | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0Eh | Timer Control | TE | X | X | X | X | X | TD | |
| | Reset | 0 | X | X | X | X | X | 1 | 1 |

| Bit | Symbol | Value | Description |
|---|---|---|---|
| 7 | TE | Periodic Countdown Timer Enable bit. This bit controls the start/stop setting for the Periodic Countdown Timer Interruption function. | |
| | | 0 | Stops the Periodic Countdown Timer Interrupt function. – Default value |
| | | 1 | Starts the Periodic Countdown Timer Interrupt function (a countdown starts from a preset value). |
| 6:2 | X | 0 or 1 | Unused |
| 1:0 | TD | Periodic Countdown Timer Clock Frequency (see PERIODIC COUNTDOWN TIMER INTERRUPT FUNCTION)(1) | |
| | | 00 | 4096 Hz |
| | | 01 | 64 Hz |
| | | 10 | 1 Hz |
| | | 11 | 1/60 Hz – Default value |

(1) When not in use, the TD field is recommended to be set to 11 (1⁄60 Hz) for power saving.

### 0Fh – Timer Value

This register holds the current value of the Periodic Countdown Timer. It may be loaded with the desired starting value when the Periodic Countdown Timer is stopped.

| Address | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0Fh | Timer Value | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 |
| | Reset | X | X | X | X | X | X | X | X |

| Bit | Symbol | Value | Description |
|---|---|---|---|
| 7:0 | Timer Value | 00h to FFh | Periodic Countdown Timer Value (see PERIODIC COUNTDOWN TIMER INTERRUPT FUNCTION) |

Countdown Period in seconds:

$$\text{Countdown Period} = \frac{\text{Timer Value}}{\text{Timer Clock Frequency}}$$

## 3.7. REGISTER RESET VALUES SUMMARY

| Address | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 00h | Control1 | 0 | 0 | 0 | 0 | 1[(1)] | 0 | 0 | 0 |
| 01h | Control2 | 1[(1)] | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 02h | Seconds | 1 | X | X | X | X | X | X | X |
| 03h | Minutes | X | X | X | X | X | X | X | X |
| 04h | Hours | X | X | X | X | X | X | X | X |
| 05h | Date | X | X | X | X | X | X | X | X |
| 06h | Weekdays | X | X | X | X | X | X | X | X |
| 07h | Months / Century | X | X | X | X | X | X | X | X |
| 08h | Years | X | X | X | X | X | X | X | X |
| 09h | Minutes Alarm | 1 | X | X | X | X | X | X | X |
| 0Ah | Hours Alarm | 1 | X | X | X | X | X | X | X |
| 0Bh | Date Alarm | 1 | X | X | X | X | X | X | X |
| 0Ch | Weekday Alarm | 1 | X | X | X | X | X | X | X |
| 0Dh | CLKOUT Frequency | 1 | X | X | X | X | X | 0 | 0 |
| 0Eh | Timer Control | 0 | X | X | X | X | X | 1 | 1 |
| 0Fh | Timer Value | X | X | X | X | X | X | X | X |

Bit positions labeled as X are undefined at power-on and unchanged by subsequent resets.
(1) Should always be written with logic 0 (TESTC Bit and N Bit).

RV-8564-C3 resets to:

- Time (hh:mm:ss) = XX:XX:XX
- Date (YY-MM-DD) = XX-XX-XX
- Weekday = X
- Century Bit = X
- N Bits = X (should always be written with logic 0)
- TESTC Bit = 1 (must be set to logic 0 for normal operations)
- Pins = CLKOUT Frequency = 32.768 kHz (when CLKOE is HIGH)
- Alarms = disabled
- Timer = disabled, Timer Clock Frequency = 1/60 Hz
- Interrupts = disabled
- Voltage Low Flag = 1 (can be cleared by writing a 0 to the bit)

# 4. DETAILED FUNCTIONAL DESCRIPTION

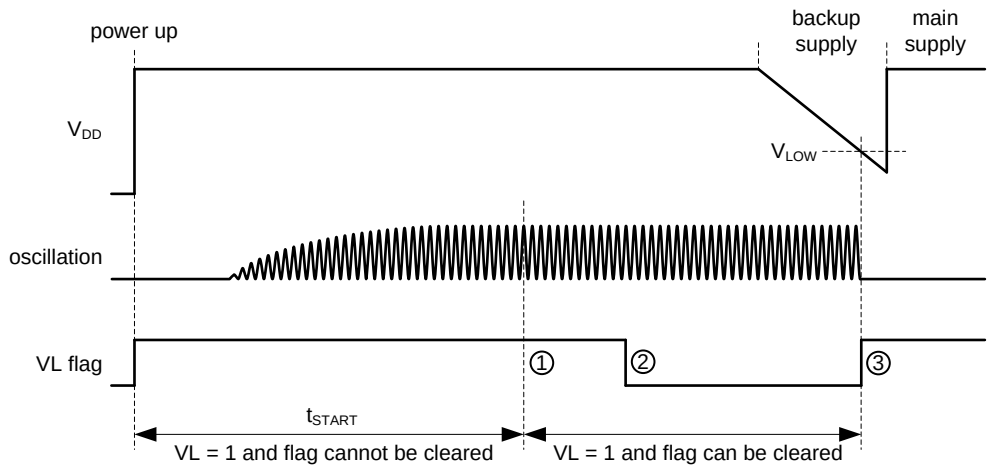
## 4.1. POWER ON RESET (POR)

The power on reset (POR) is generated at start-up. All registers including the Counter Registers are initialized to their reset values (see REGISTER RESET VALUES SUMMARY).

## 4.2. VOLTAGE LOW FLAG

The RV-8564-C3 has an on-chip voltage low detector. When $V_{DD}$ drops below $V_{LOW}$ the VL (Voltage Low) flag is set to indicate that the integrity of the clock information is no longer guaranteed. The VL flag can only be cleared by command.

VL flag:

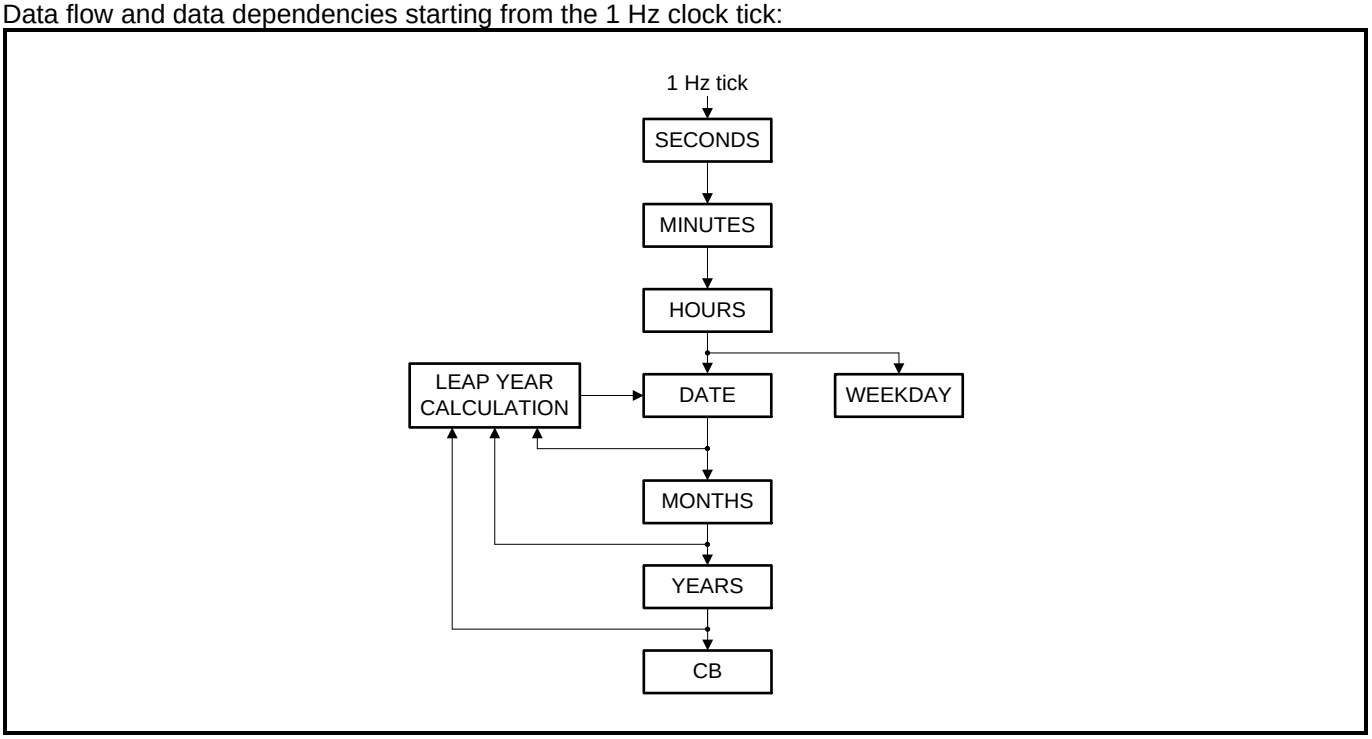



① Oscillation now stable.
② VL flag cleared by software.
③ VL flag set when $V_{DD}$ drops below $V_{LOW}$.

The VL flag is intended to detect the situation when $V_{DD}$ is decreasing slowly, for example under battery operation. Should the oscillator stop or $V_{DD}$ reach $V_{LOW}$ before power is reasserted, then the VL flag will be set. This indicates that the time is possibly corrupted.

## 4.3. SETTING AND READING THE TIME

Data flow and data dependencies starting from the 1 Hz clock tick:



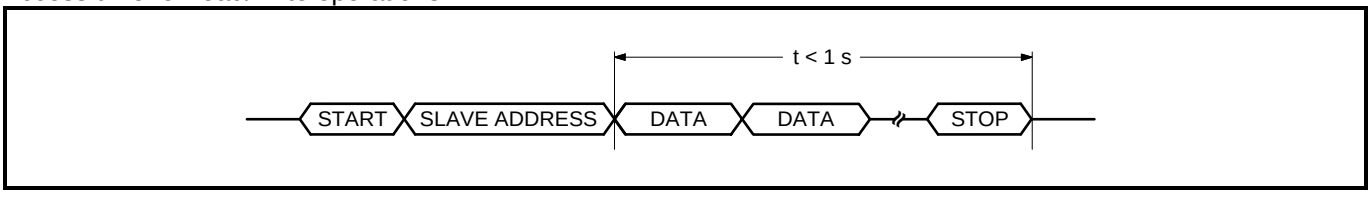

During read/write operations, the time counting registers (memory locations 02h through 08h) are frozen for 1 second.

The freezing prevents:

- Faulty reading of the clock and calendar during a carry condition
- Incrementing the time registers during the read cycle

When the read/write access has been terminated within 1 second (t < 1 s), the time circuit is de-frozen immediately and any pending request to increment the time counters that occurred during the read/write access is correctly applied. Maximal one 1 Hz tick can be handled.
When the read/write access last longer than 1 second, the time circuit is de-frozen automatically after another second in order not to miss further 1 Hz ticks and the one lost 1 Hz tick cannot be handled completely. Therefore, each interface communication has to be correctly terminated within 1 second (see following Figure).

Access time for read/write operations:



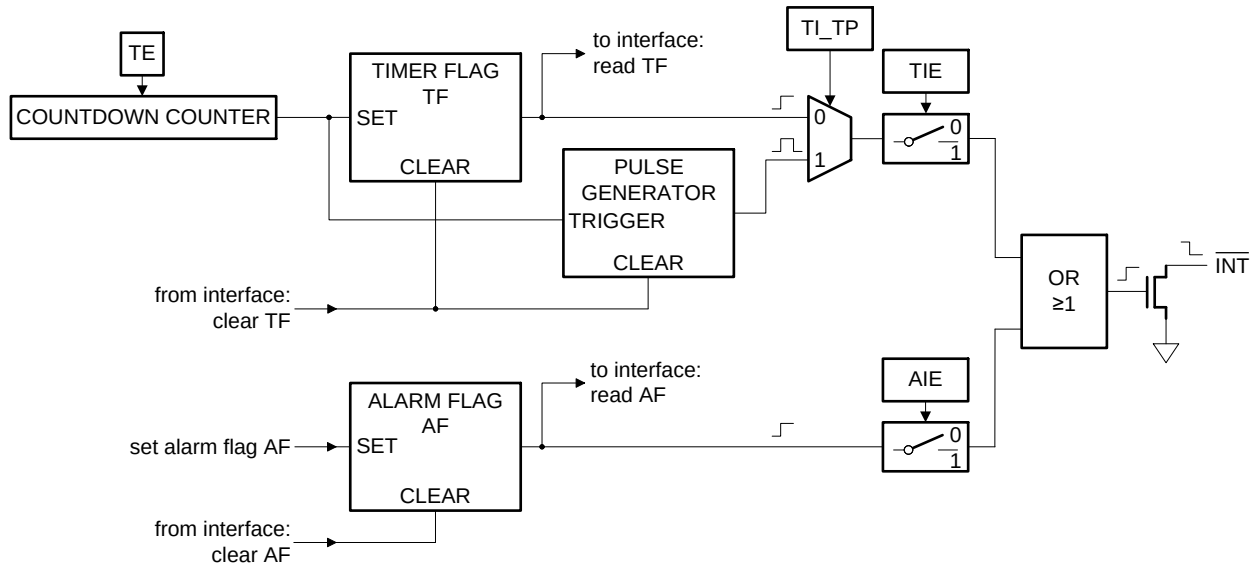

Because of this method, it is very important to make a read or write access in one go, that is, setting or reading seconds through to years should be made in one single access. Failing to comply with this method could result in the time becoming corrupted (see also FREEZE AND BUS TIMEOUT FUNCTION).

## 4.4. INTERRUPT OUTPUT

The interrupt pin $\overline{INT}$ can be triggered by two different functions:

- ALARM FUNCTION
- PERIODIC COUNTDOWN TIMER INTERRUPT FUNCTION

Interrupt scheme:




When bits TIE and AIE are disabled, pin $\overline{INT}$ will remain high-impedance.

### 4.4.1.SERVICING INTERRUPTS

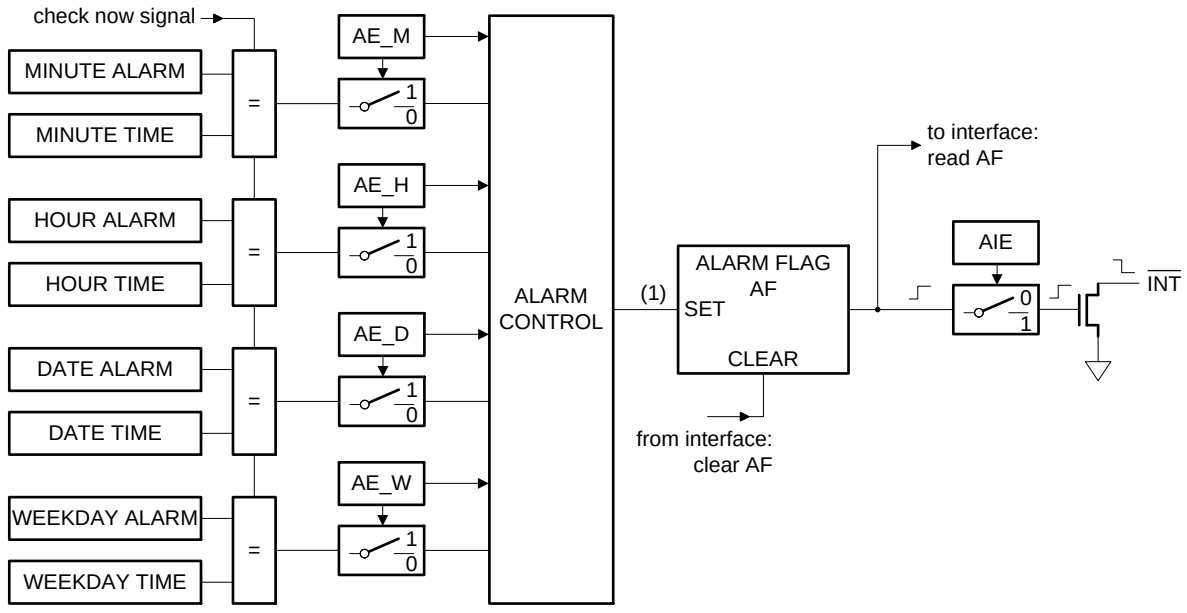
The $\overline{INT}$ pin can indicate two types of interrupts. It outputs the logic OR operation result of these interrupt outputs. When an interrupt is detected, (when the $\overline{INT}$ pin is at low level), the TF and AF flags can be read to determine which interrupt event has occurred.
The $\overline{INT}$ pin is always connected to the OR'ed flag signals and cannot be disconnected separately. To check whether an event has occurred without monitoring the $\overline{INT}$ pin, software can read the TF and AF interrupt flags (polling).

## 4.5. ALARM FUNCTION

By clearing the alarm enable bit (AE_x) of one or more of the alarm registers, the corresponding alarm condition(s) are active. When an alarm occurs, AF is set logic 1. The asserted AF can be used to generate an interrupt ($\overline{INT}$). The AF is cleared by command.

The registers at addresses 09h through 0Ch contain alarm information. When one or more of these registers is loaded with minute, hour, date or weekday, and its corresponding AE_x is logic 0, then that information is compared with the current minute, hour, date, and weekday. When all enabled comparisons first match, the Alarm Flag (AF in CONTROL REGISTERS, 01h – Control2) is set logic 1.

Alarm function block diagram:




(1) Only when all enabled alarm settings are matching.
It is only on increment to a matched case that the Alarm Flag is set.

### 4.5.1.ALARM INTERRUPT

The generation of interrupts from the alarm function is controlled via bit AIE. If bit AIE is set to 1, the $\overline{INT}$ pin follows the condition of bit AF. AF remains set until cleared by command. Once AF has been cleared, it will only be set again when the time increments to match the alarm condition once more. Alarm registers which have their AE_x bit at logic 1 are ignored.

### 4.5.2.USE OF THE ALARM INTERRUPT

The following bits and registers are related to the Alarm Interrupt function:

- AIE bit and AF flag in Control2 Register (01h) (see CONTROL REGISTERS)
- Minutes Register (03h) (see TIME AND DATE REGISTERS)
- Hours Register (04h) (see TIME AND DATE REGISTERS)
- Date Register (05h) (see TIME AND DATE REGISTERS)
- Weekdays Register (06h) (see TIME AND DATE REGISTERS)
- Minutes Alarm Register and AE_M bit (09h) (see ALARM REGISTERS)
- Hours Alarm Register and AE_H bit (0Ah) (see ALARM REGISTERS)
- Date Alarm Register and AE_D bit (0Bh) (see ALARM REGISTERS)
- Weekday Alarm Register and AE_W bit (0Ch) (see ALARM REGISTERS)

Prior to entering any timer settings for the Alarm Interrupt, it is recommended to write a 0 to the AIE bit to prevent inadvertent interrupts on $\overline{INT}$ pin. When the Alarm Interrupt function is not used, the 4 Bytes of the Alarm registers (09h, 0Ah, 0Bh and 0Ch) can be used as RAM bytes. In such case, be sure to write a 0 to the AIE bit (if the AIE bit value is 1 and the Alarm registers are used as RAM registers, $\overline{INT}$ may change to low level unintentionally).

Procedure to use the Alarm Interrupt function:

1. Initialize bits AE_M, AE_H, AE_D and AE_W to 1 (1 = disabled).
2. Initialize bits AIE and AF to 0.
3. Write the desired alarm settings in registers 09h, 0Ah, 0Bh and 0Ch. The four alarm enable bits, AE_M, AE_H, AE_D and AE_W, are used to select the corresponding register that has to be taken into account for match or not (hours in 24-hour format). See the following table.
4. Set the AIE bit to 1 if you want to get a hardware interrupt on $\overline{INT}$ pin.

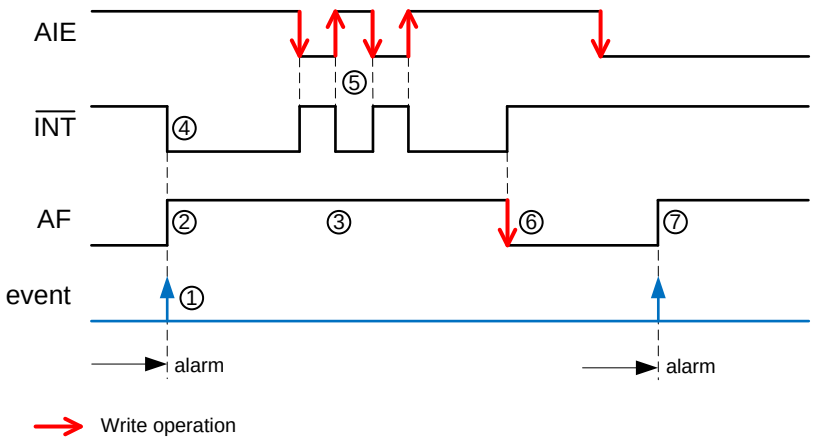
Alarm Interrupt:

| Alarm enable bits | | | | Alarm event |
|---|---|---|---|---|
| AE_W | AE_D | AE_H | AE_M | |
| 0 | 0 | 0 | 0 | When minutes, hours, date and weekday match(1) |
| 0 | 0 | 0 | 1 | When hours, date and weekday match(1) |
| 0 | 0 | 1 | 0 | When minutes, date and weekday match(1) |
| 0 | 0 | 1 | 1 | When weekday and date match(1) |
| 0 | 1 | 0 | 0 | When weekday, hours and minutes match (once per week)(1) |
| 0 | 1 | 0 | 1 | When weekday and hours match (once per week)(1) |
| 0 | 1 | 1 | 0 | When weekday and minutes match (every hour at the specified weekday)(1) |
| 0 | 1 | 1 | 1 | When weekday match (once per week)(1) |
| 1 | 0 | 0 | 0 | When date, hours and minutes match (once per month)(1) |
| 1 | 0 | 0 | 1 | When date and hours match (once per month)(1) |
| 1 | 0 | 1 | 0 | When date and minutes match (every hour at the specified date)(1) |
| 1 | 0 | 1 | 1 | When date match (once per month)(1) |
| 1 | 1 | 0 | 0 | When hours and minutes match (once per day)(1) |
| 1 | 1 | 0 | 1 | When hours match (once per day)(1) |
| 1 | 1 | 1 | 0 | When minutes match (once per hour)(1) |
| 1 | 1 | 1 | 1 | No alarm interrupt event will occur(1) – Default value |

(1) AE_x bits (where x is M, H, D and W)
AE_x = 0: Alarm is enabled
AE_x = 1: Alarm is disabled

### 4.5.3.ALARM DIAGRAM

Diagram of the Alarm Interrupt function:




① An Alarm Interrupt event occurs when the selected Alarm registers match the respective counters.

② When an Alarm Interrupt event occurs, the AF flag is set to 1.

③ The AF bit retains 1 until it is cleared to 0 by software.

④ If the AIE bit is 1 and an Alarm Interrupt occurs, the $\overline{INT}$ pin output goes low.

⑤ If the AIE value is changed from 1 to 0 while the $\overline{INT}$ pin output is low, the $\overline{INT}$ pin immediately changes its status. While the AF bit value is 1, the $\overline{INT}$ status can be controlled by the AIE bit.

⑥ If the $\overline{INT}$ pin is low, its status changes as soon as the AF bit value is cleared from 1 to 0.

⑦ If the AIE bit value is 0 when an Alarm Interrupt occurs, the $\overline{INT}$ pin status does not go low.

## 4.6. PERIODIC COUNTDOWN TIMER INTERRUPT FUNCTION

The 8-bit Timer Value Register (0Fh) is controlled by the Timer Control register (0Eh) with the TD field (bits 1:0) that determines one of 4 Timer Clock Frequencies (4096 Hz, 64 Hz, 1 sec, or 1/60 Hz) and with the enable / disable bit TE (bit 7). When enabled with TE, the timer counts down from the software loaded 8-bit binary Timer Value. At the end of every countdown, the timer sets the Timer Flag TF (Control2 register 01h, bit 2) to logic 1. The TF flag may only be cleared using the interface.

The generation of interrupts from the periodic countdown timer function is controlled via enable bit TIE (Control2 register 01h, bit 0) and the mode control bit TI_TP (Control2 register 01h, bit 4). If bit TIE is enabled and the interrupt is in Interval Mode (TI_TP = 0) the signal on $\overline{INT}$ pin is generated as a permanent active signal which follows the condition of the Timer Flag TF. If bit TIE is enabled and the interrupt is in Pulse Mode (TI_TP = 1) the interrupt may be generated as a pulsed signal every countdown period.

When reading the Timer Value, the current countdown value is returned and not the preset value (reload value). For accurate reading back of this value, I²C-bus clock (SDA) must be operating at a frequency of at least twice the selected Timer Clock Frequency. Since it is not possible to freeze the countdown timer counter during read back, it is recommended to read the register twice and check for consistent results.

### 4.6.1.PERIODIC COUNTDOWN TIMER FLAG TF

The Periodic Countdown Timer Flag (bit TF) is set logic 1 on the first trigger of the Periodic Countdown Timer Interrupt. The purpose of the flag is to allow the controlling system to interrogate what caused the interrupt: Timer or Alarm. The flag can be read and cleared by command.
The status of the Periodic Countdown Timer Flag TF can affect the $\overline{INT}$ pulse generation ($t_{RTN}$) depending on the setting of TI_TP (see CONTROL REGISTERS, 01h – Control2):

### 4.6.2.PERIODIC COUNTDOWN TIMER INTERRUPT MODE TI_TP

When Interrupt is in Interval Mode (TI_TP = 0):

- when TF is not cleared, only one Interrupt after the first countdown occurs
- the $\overline{INT}$ generation follows the TF flag
- TF stays set until it is cleared
- if TF is not cleared before the next coming interrupt, no $\overline{INT}$ is generated

When Interrupt is in Pulse Mode (TI_TP = 1):

- the Periodic Countdown Timer runs in a repetitive loop and keeps generating periodic interrupts
- an $\overline{INT}$ pulse is generated independent of the status of the Periodic Countdown Timer Flag TF
- TF stays set until it is cleared.
- TF does not affect $\overline{INT}$

### 4.6.3.PULSE GENERATOR

When the Timer Pulse Mode is activated (TI_TP = 1) the Pulse Generator for the Periodic Countdown Timer Interrupt uses an internal clock and is dependent on the selected Timer Clock Frequency for the countdown timer and on the Timer Value. As a consequence, the width of the interrupt pulse ($t_{RTN}$) varies (see following Table). TF and $\overline{INT}$ become active simultaneously.

$\overline{INT}$ pulse width $t_{RTN}$ when using the Periodic Countdown Timer:

| TD | Timer Clock Frequency | $\overline{INT}$ pulse width $t_{RTN}$. | |
|---|---|---|---|
| | | Timer Value = 1[1] | Timer Value > 1[1] |
| 00 | 4096 Hz | 122 µs | 244 µs |
| 01 | 64 Hz | 7.813 ms | 15.625 ms |
| 10 | 1 Hz | 15.625 ms | 15.625 ms |
| 11 | 1/60 Hz | 15.625 ms | 15.625 ms |

[1] Timer Value = loaded countdown value. Timer stops when Timer Value = 0.

### 4.6.4.TIMER VALUE

The timer has four selectable Timer Clock Frequencies (TD) allowing Countdown Periods in the range from 244 µs to 255 min (4 hours 15 min). When periods longer than 4 hours are required, the alarm function can be used.

Countdown Period in seconds:

$$\text{Countdown Period} = \frac{\text{Timer Value}}{\text{Timer Clock Frequency}}$$

Countdown Period:

| Timer Value | Countdown Period | | | |
|---|---|---|---|---|
| | TD = 00 (4096 Hz) | TD = 01 (64 Hz) | TD = 10 (1 Hz) | TD = 11 (1/60 Hz) (1) |
| 0 | - | - | - | - |
| 1 | 244.14 µs | 15.625 ms | 1 s | 1 min |
| 2 | 488.28 µs | 31.250 ms | 2 s | 2 min |
| 3 | 732.42 µs | 46.875 ms | 3 s | 3 min |
| : | : | : | : | : |
| 255 (FFh) | 62.26 ms | 3.984 s | 255 s | 255 min |

(1) When not in use, the TD field is recommended to be set to 11 (1/60 Hz) for power saving.

Note that all timings are generated from the 32.768 kHz oscillator and therefore, based on the frequency characteristics specified for the device, have a temperature profile with a parabolic frequency deviation which can result in a change of up to 150 ppm across the entire operating temperature range of -40°C to 85°C (max. ± 20 ppm at 25°C).

The timer counts down from the software-loaded 8-bit binary Timer Value in register 0Fh. Timer Values from 1 to 255 are valid. Loading the counter with 0 stops the timer.
When the counter decrements from 1, the Periodic Countdown Timer Flag (bit TF in register Control2) is set and the counter automatically re-loads and starts the next timer period.

If a new Timer Value is written before the end of the current timer period, then this value takes immediate effect. It is not recommended changing the Timer Value without first disabling the counter by setting bit TE logic 0. The update of the Timer Value is asynchronous to the Timer Clock Frequency.
Therefore changing it without setting bit TE logic 0 may result in a corrupted value loaded into the countdown counter. This results in an undetermined countdown period for the first period. The Timer Value will, however, be correctly stored and correctly loaded on subsequent timer periods.

### 4.6.5.USE OF THE PERIODIC COUNTDOWN TIMER

The following bits, fields and registers are related to the Periodic Countdown Timer Interrupt function:

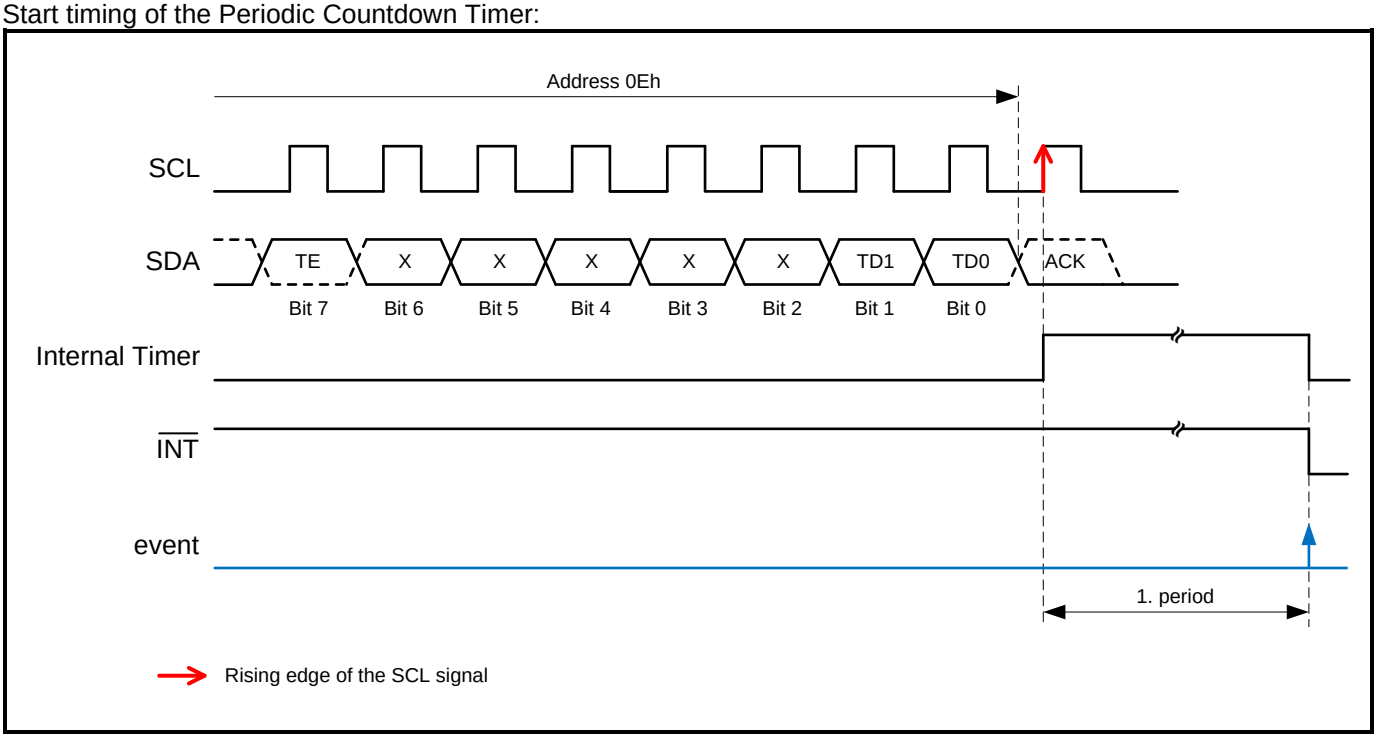
- TI_TP bit, TF flag and TIE bit (see CONTROL REGISTERS, Control2 (01h))
- TE bit and TD field (see PERIODIC COUNTDOWN TIMER CONTROL REGISTERS, Timer Control (0Eh))
- Timer Value Register (0Fh) (see PERIODIC COUNTDOWN TIMER CONTROL REGISTERS)

Prior to entering any timer settings for the Periodic Countdown Timer Interrupt function, it is recommended to write a 0 to the TE, TIE and TF bits in that order to prevent inadvertent interrupts on $\overline{INT}$ pin. When the Periodic Countdown Timer Interrupt function is not used, the Timer Value Register (0Fh) can be used as 1 Byte of RAM. The Timer Clock Frequency selection field TD is used to set the countdown period (source clock) for the Periodic Countdown Timer Interrupt function (four settings are possible).

Procedure to use the Periodic Countdown Timer Interrupt function:

1. Initialize bits TE, TIE and TF to 0. In that order, to prevent inadvertent interrupts on $\overline{INT}$ pin.
2. Choose the Timer Clock Frequency and write the corresponding value in the TD field.
3. Choose the Countdown Period based on the Timer Clock Frequency, and write the corresponding preset value to the Timer Value Register (0Fh) (see TIMER VALUE).
4. Set the TIE bit to 1 if you want to get a hardware interrupt on $\overline{INT}$ pin.
5. When interrupt on $\overline{INT}$ pin is used, choose Interval or Pulse Mode with bit TI_TP.
6. Set the TE bit from 0 to 1 to start the Periodic Countdown Timer. The countdown starts at the rising edge of the SCL signal after Bit 0 of the Address 0Eh is transferred. The following Figure shows the countdown start timing.

Start timing of the Periodic Countdown Timer:



### 4.6.6.FIRST PERIOD DURATION

When the TF flag is set, an interrupt signal on $\overline{INT}$ is generated if this mode is enabled. See Section INTERRUPT OUTPUT for details on how the interrupt can be controlled.

When starting the timer for the first time, the first period has an uncertainty. The uncertainty is a result of the enable instruction being generated from the interface clock which is asynchronous from the Timer Clock Frequency. Subsequent timer periods do not have such deviation. The amount of deviation for the first timer period depends on the chosen source clock, see following Table.

First period duration for Timer Value n(1):

| TD | Timer Clock Frequency | First period duration | | Subsequent periods duration |
|---|---|---|---|---|
| | | Minimum Period | Maximum Period | |
| 00 | 4096 Hz | (n – 1) * 244 µs + 122 µs | n * 244 µs + 122 µs | n * 244 µs |
| 01 | 64 Hz | (n – 1) * 15.625 ms | n * 15.625 ms | n * 15.625 ms |
| 10 | 1 Hz | (n – 1) * 1 s | n * 1 s | n * 1 s |
| 11 | 1/60 Hz | n * 60 s - 1 s | n * 60 s | n * 60 s |

(1) Timer Values n from 1 to 255 are valid. Loading the counter with 0 stops the timer.

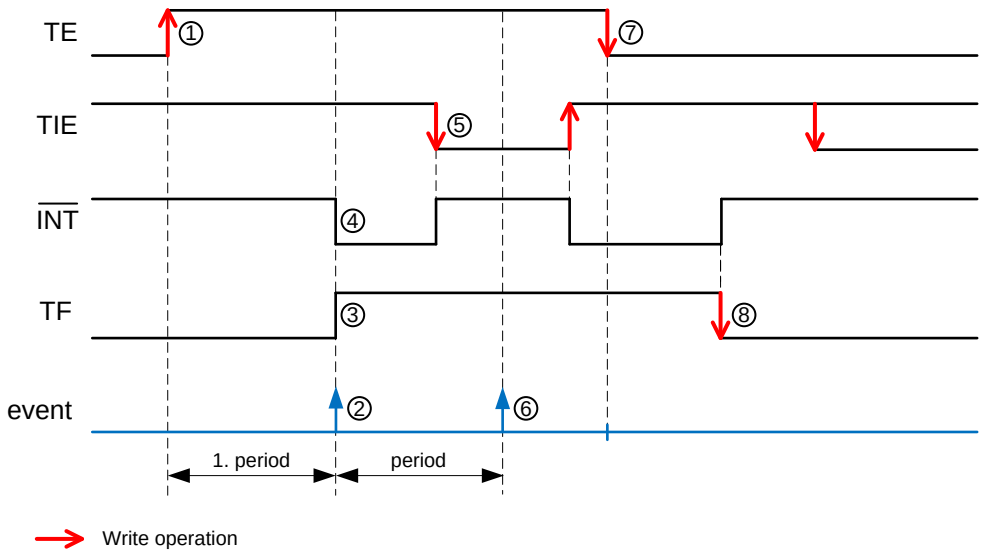
At the end of every countdown, the timer sets the Periodic Countdown Timer Flag (bit TF in register Control2). Bit TF can only be cleared by command. The asserted bit TF can be used to generate an interrupt at pin $\overline{INT}$. The interrupt may be generated as a pulsed signal every countdown period or as a permanently active signal which follows the condition of bit TF. Bit TI_TP is used to control this mode selection and the interrupt output may be disabled with bit TIE (see CONTROL REGISTERS, 01h – Control2; and Figure “General countdown timer behavior” above).

When reading the Timer Value, the current countdown value is returned and **not** the initial Timer Value. Since it is not possible to freeze the countdown timer counter during read back, it is recommended to read the register twice and check for consistent results.

### 4.6.7.INTERVAL MODE DIAGRAM (TI_TP = 0)

In this mode only one Interrupt on $\overline{INT}$ occurs when TF is not cleared.

Diagram of the Periodic Countdown Timer Interrupt function in Interval Mode (TI_TP = 0):




① The Periodic Countdown Timer starts from the preset Timer Value when writing a 1 to the TE bit. The countdown is based on the Timer Clock Frequency.

② When the Timer Value reaches 00h, an interrupt event occurs. After the interrupt, the counter is automatically reloaded with the preset Timer Value, and starts again the countdown.

③ When a Periodic Countdown Timer Interrupt occurs, the TF flag is set to 1.

④ If the TIE bit is 1 and a Periodic Countdown Timer Interrupt occurs, the $\overline{INT}$ pin output goes low.

⑤ If the TIE value is changed from 1 to 0 while the $\overline{INT}$ pin output is LOW, the $\overline{INT}$ pin immediately changes its status. While the TF flag value is 1, the $\overline{INT}$ status can be controlled by the TIE bit.

⑥ No interrupt is created because TIE bit is 0. And the TF flag can't show the interrupt event because it was not cleared to 0 before.

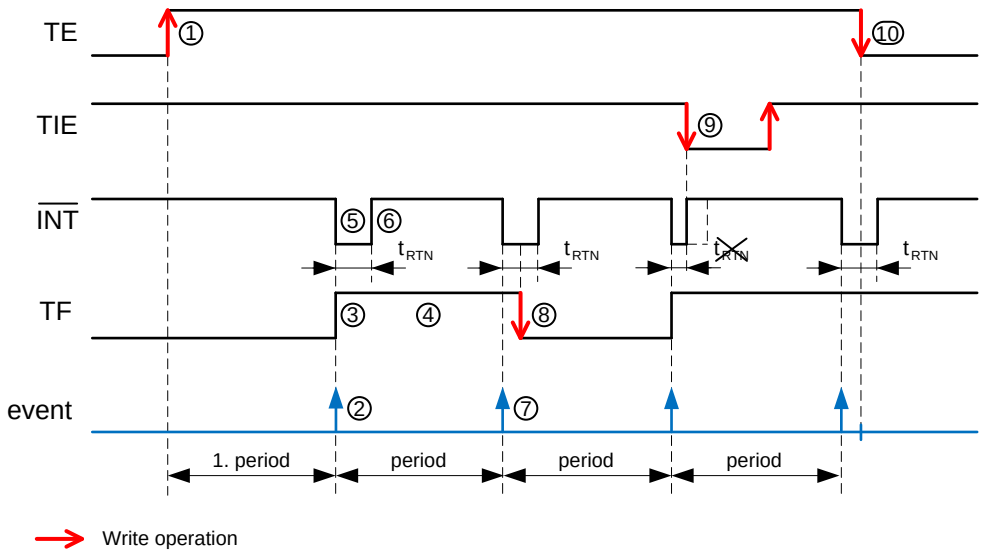
⑦ When the TE bit is cleared to 0 the countdown is stopped. The TF bit value is retained at 1 and the $\overline{INT}$ pin status is not reset. The TF flag retains 1 until it is cleared to 0 by software.

⑧ When the TF flag is cleared to 0, the $\overline{INT}$ pin is disabled (goes high) regardless of TE bit's value.

### 4.6.8.PULSE MODE DIAGRAM (TI_TP = 1)

In this mode periodic interrupt pulses on $\overline{INT}$ are generated independent of the status of TF.

Diagram of the Periodic Countdown Timer Interrupt function in Pulse Mode (TI_TP = 1):




① The Periodic Countdown Timer starts from the preset Timer Value when writing a 1 to the TE bit. The countdown is based on the Timer Clock Frequency.

② When the Timer Value reaches 00h, an interrupt event occurs. After the interrupt, the counter is automatically reloaded with the preset Timer Value, and starts again the countdown.

③ When a Periodic Countdown Timer Interrupt occurs, the TF flag is set to 1.

④ The TF flag retains 1 until it is cleared to 0 by software.

⑤ If the TIE bit is 1 and a Periodic Countdown Timer Interrupt occurs, the $\overline{INT}$ pin output goes low.

⑥ The $\overline{INT}$ pin output remains LOW during the Auto reset time $t_{RTN}$, and then it is automatically cleared to 1. The TD field determines the Timer Clock Frequency and the Auto reset time $t_{RTN}$ (see PULSE GENERATOR).

⑦ When the next interrupt event occurs, the $\overline{INT}$ is again set to LOW level. Since the TF flag was not cleared to 0 previously, it retains 1.

⑧ If the $\overline{INT}$ pin is LOW level during the $t_{RTN}$ period, its status does not change when the TF flag value is cleared to 0.

⑨ If the $\overline{INT}$ pin is LOW, its status changes as soon as the TIE bit value is cleared to 0.

⑩ When a 0 is written to the TE bit, the Periodic Countdown Timer function is stopped and the $\overline{INT}$ pin is cleared after the Auto reset time $t_{RTN}$. The TF flag retains 1 until it is cleared to 0 by software.

## 4.7. CLKOUT FREQUENCY SELECTION

A programmable square wave is available at pin CLKOUT. Operation is controlled by the FD field in the register CLKOUT Frequency. Frequencies of 32.768 kHz (default), 1024 Hz, 32 Hz and 1 Hz can be generated for use as a system clock, microcontroller clock, input to a charge pump, or for calibration of the crystal oscillator.

Pin CLKOUT is a push-pull output and enabled at power-on (when CLKOE is HIGH). CLKOUT can be disabled by clearing bit FE or by setting CLKOE pin LOW. When disabled, the CLKOUT pin is LOW.

The duty cycle of the selected clock is not controlled. However, due to the nature of the clock generation, all are 50 : 50 except the 32.768 kHz frequency.

The STOP bit function can also affect the CLKOUT signal, depending on the selected frequency. When the STOP bit is set logic 1, the CLKOUT pin generates a continuous LOW for those frequencies that can be stopped (for more details, see STOP BIT FUNCTION).

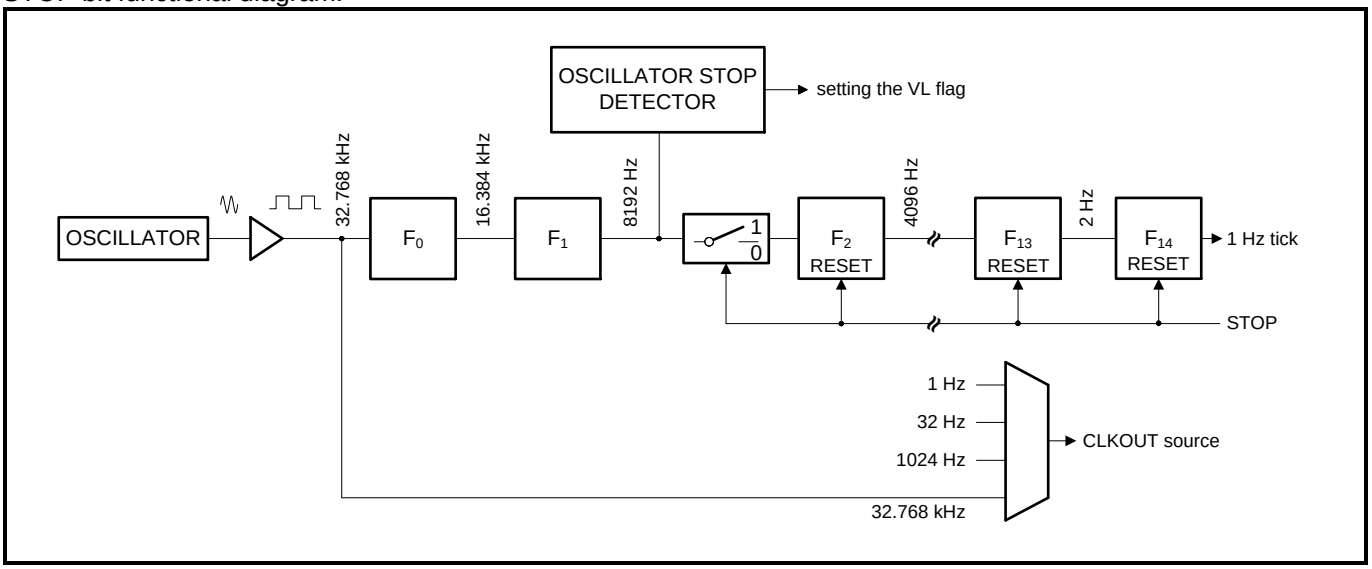
| FD | CLKOUT Frequency | Typical duty cycle | Effect of STOP bit |
|---|---|---|---|
| 00 | 32.768 kHz – Default value | 50 ±10 % | no effect |
| 01 | 1024 Hz | 50 % | CLKOUT = LOW |
| 10 | 32 Hz | 50 % | CLKOUT = LOW |
| 11 | 1 Hz | 50 % | CLKOUT = LOW |

## 4.8. STOP BIT FUNCTION

The function of the STOP bit is to allow for accurate starting of the time circuits.

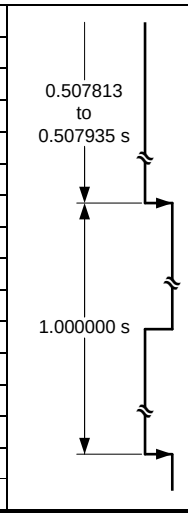
The STOP bit function causes the upper part of the prescaler ($F_2$ to $F_{14}$) to be held in reset and thus no 1 Hz ticks are generated. The STOP bit function will not affect the CLKOUT of 32.768 kHz, but will stop the generation of 1024 Hz, 32 Hz and 1 Hz (see also CLKOUT FREQUENCY SELECTION).

STOP bit functional diagram:




The time circuits can then be set and do not increment until the STOP bit is released (see following Table and Figure).

First increment of time circuits after STOP bit release:

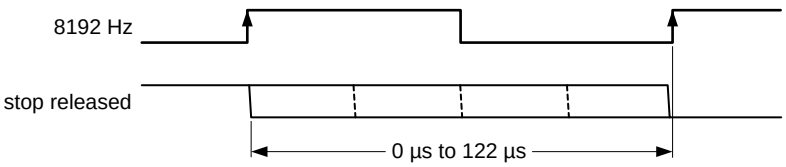
| STOP bit | Prescaler bits [1] $F_0F_1$-$F_2$ to $F_{14}$ | 1 Hz tick | Time hh:mm:ss | Comment |
|---|---|---|---|---|
| Clock is running normally | | | | |
| 0 | 01-0 0001 1101 0100 | | 12:45:12 | Prescaler counting normally |
| STOP bit is activated by user. $F_0F_1$ are not reset and values cannot be predicted externally | | | | |
| 1 | XX-0 0000 0000 0000 | | 12:45:12 | Prescaler is reset; time circuits are frozen |
| New time is set by user | | | | |
| 1 | XX-0 0000 0000 0000 | | 08:00:00 | Prescaler is reset; time circuits are frozen |
| STOP bit is released by user | | | | |
| 0 | XX-0 0000 0000 0000 |  | 08:00:00 | Prescaler is now running |
| | XX-1 0000 0000 0000 | | 08:00:00 | - |
| | XX-0 1000 0000 0000 | | 08:00:00 | - |
| | XX-1 1000 0000 0000 | | 08:00:00 | - |
| | : | | : | : |
| | 11-1 1111 1111 1110 | | 08:00:00 | - |
| | 00-0 0000 0000 0001 | | 08:00:01 | 0 to 1 transition of $F_{14}$ increments the time circuits |
| | 10-0 0000 0000 0001 | | 08:00:01 | - |
| | : | | : | : |
| | 11-1 1111 1111 1111 | | 08:00:01 | - |
| | 00-0 0000 0000 0000 | | 08:00:01 | - |
| | 10-0 0000 0000 0000 | | 08:00:01 | - |
| | : | | : | : |
| | 11-1 1111 1111 1110 | | 08:00:01 | - |
| | 00-0 0000 0000 0001 | | 08:00:02 | 0 to 1 transition of $F_{14}$ increments the time circuits |
| | 10-0 0000 0000 0001 | | 08:00:02 | - |



1) $F_0$ is clocked at 32.768 kHz.

The lower two stages of the prescaler ($F_0$ and $F_1$) are not reset. And because the I²C-bus is asynchronous to the crystal oscillator, the accuracy of restarting the time circuits is between zero and one 8192 Hz cycle (see following Figure).

STOP bit release timing:




The first increment of the time circuits is between 0.507813 s and 0.507935 s after STOP bit is released. The uncertainty is caused by the prescaler bits $F_0$ and $F_1$ not being reset (see Table above) and the unknown state of the 32.768 kHz clock.

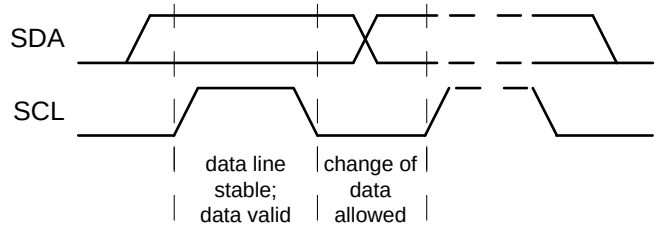
# 5. I²C-BUS INTERFACE

The I²C-bus interface is for bidirectional, two-line communication between different ICs or modules. The RV-8564-C3 is accessed at addresses A2h/A3h, and supports Fast Mode (up to 400 kHz). The I²C-bus interface consists of two lines: one bi-directional data line (SDA) and one clock line (SCL). Both lines are connected to a positive supply via pull-up resistors. Data transfer is initiated only when the interface is not busy.

## 5.1. BIT TRANSFER

One data bit is transferred during each clock pulse. The data on the SDA line remains stable during the HIGH period of the clock pulse, as changes in the data line at this time are interpreted as a control signals. Data changes should be executed during the LOW period of the clock pulse (see Figure below).

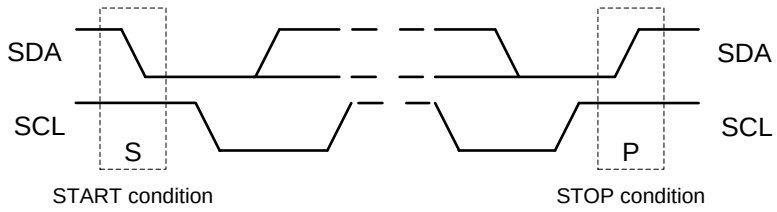
Bit transfer:




## 5.2. START AND STOP CONDITIONS

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the START condition (S). A LOW-to-HIGH transition of the data line, while the clock is HIGH, is defined as the STOP condition (P) (see Figure below).

Definition of START and STOP conditions:




A START condition which occurs after a previous START but before a STOP is called a Repeated START condition, and functions exactly like a normal STOP followed by a normal START.

**Caution:**
When communicating with the RV-8564-C3 module, the series of operations from transmitting the START condition to transmitting the STOP condition should occur **within 1 second**.
If this series of operations requires **1 second or longer**, the I²C-bus interface will be automatically cleared and set to standby mode by the bus timeout function of the RV-8564-C3 module. Note with caution that both write and read operations are invalid for communications that occur during or after this auto clearing operation (when the read operation is invalid, all data that is read has a value of FFh). Restarting of communications begins with transfer of the START condition again (see also FREEZE AND BUS TIMEOUT FUNCTION).

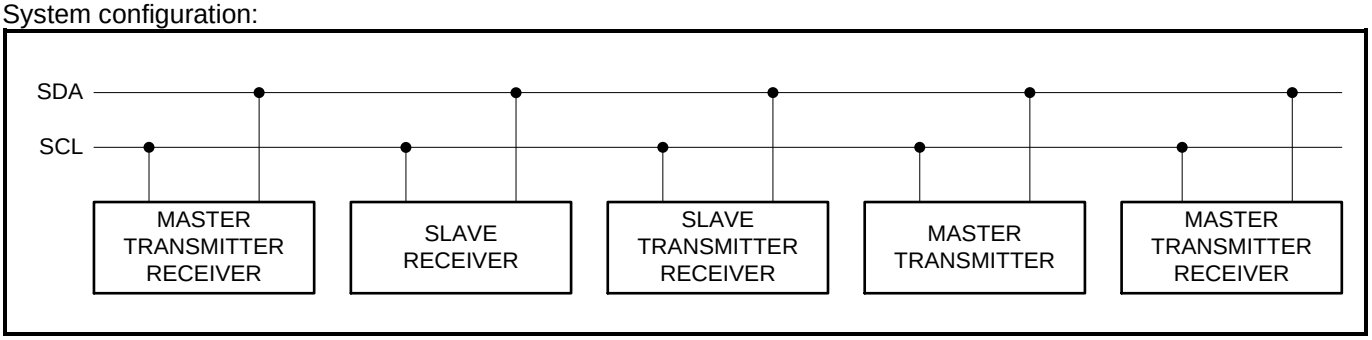
## 5.3. DATA VALID

After a START condition, SDA is stable for the duration of the high period of SCL. The data on SDA may be changed during the low period of SCL. There is one clock pulse per bit of data. Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between the START and STOP conditions is not limited (however, the transfer time must be no longer than 1 second). The information is transmitted byte-wise and each receiver acknowledges with a ninth bit.

## 5.4. SYSTEM CONFIGURATION

Since multiple devices can be connected with the I²C-bus, all I²C-bus devices have a fixed and unique device address built-in to allow individual addressing of each device.
The device that controls the I²C-bus is the Master; the devices which are controlled by the Master are the Slaves. A device generating a message is a Transmitter; a device receiving a message is the Receiver. The RV-8564-C3 acts as a Slave-Receiver or Slave-Transmitter.
Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the START procedure. The clock signal SCL is only an input signal and only generated by a Master, but the data signal SDA is a bidirectional line.

System configuration:

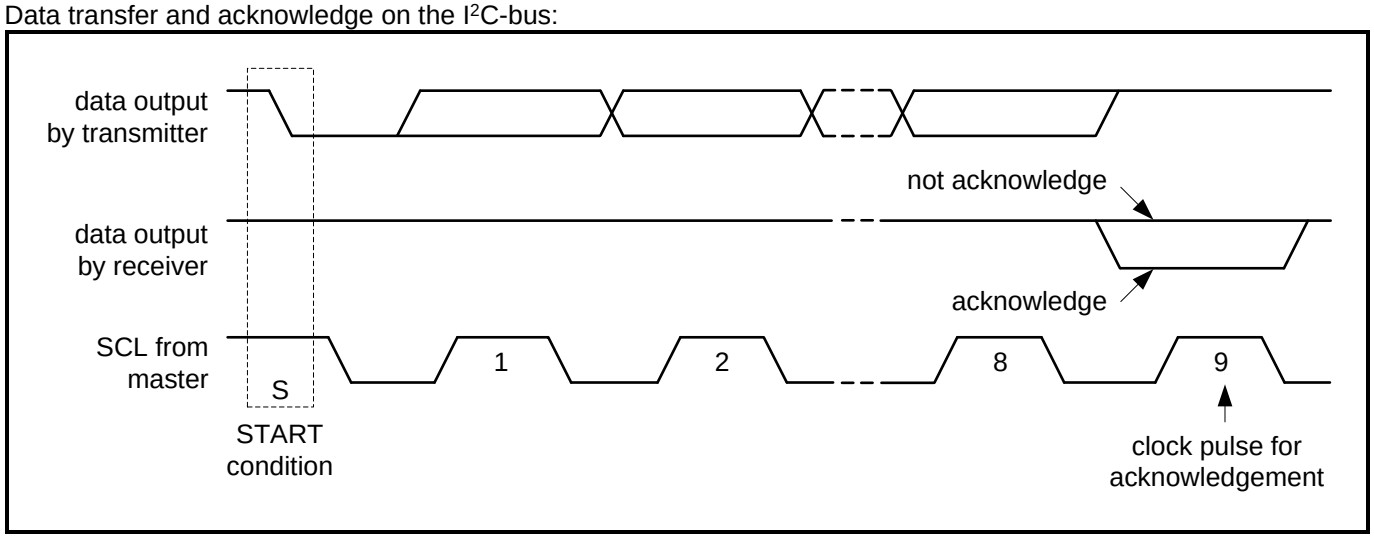


## 5.5. ACKNOWLEDGE

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited (however, the transfer time must be no longer than 1 second). Each byte of eight bits is followed by an acknowledge cycle.

- A slave receiver, which is addressed, must generate an acknowledge cycle after the reception of each byte.
- Also a master receiver must generate an acknowledge cycle after the reception of each byte that has been clocked out of the slave transmitter.
- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse (set-up and hold times must be taken into consideration).
- A master receiver must signal an end of data to the transmitter by not generating an acknowledge cycle on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

Data transfer and acknowledge on the I²C-bus:




## 5.6. SLAVE ADDRESS

On the I²C-bus the 7-bit slave address 1010001b is reserved for the RV-8564-C3. The entire I²C-bus slave address byte is shown in the following table.

| Slave address | | | | | | | R/$\overline{W}$ | Transfer data |
|---|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 ( R ) | A3h (read) |
| | | | | | | | 0 ( $\overline{W}$ ) | A2h (write) |

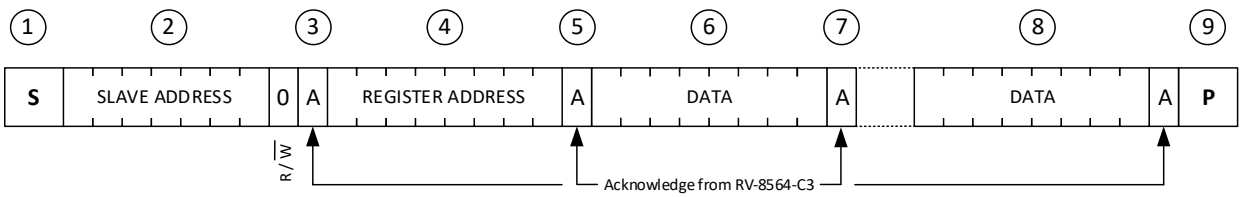
After a START condition, the I²C-bus slave address has to be sent to the RV-8564-C3 device. The R/$\overline{W}$ bit defines the direction of the following single or multiple byte data transfer. The 7-bit address is transmitted MSB first. If this address is 1010001b, the RV-8564-C3 is selected, the eighth bit indicates a read (R/$\overline{W}$ = 1) or a write (R/$\overline{W}$ = 0) operation (results in A3h or A2h) and the RV-8564-C3 supplies the ACK. The RV-8564-C3 ignores all other address values and does not respond with an ACK.
In the write operation, a data transfer is terminated by sending either the STOP condition or the START condition of the next data transfer.

## 5.7. WRITE OPERATION

Master transmits to Slave-Receiver at specified address. The Register Address is an 8-bit value that defines which register is to be accessed next. The actual Register Address complies with the lower 4-bit value. The upper four bits of the Register Address are not used. After writing one byte, the Register Address is automatically incremented by 1.

Master writes to slave RV-8564-C3 at specific address:

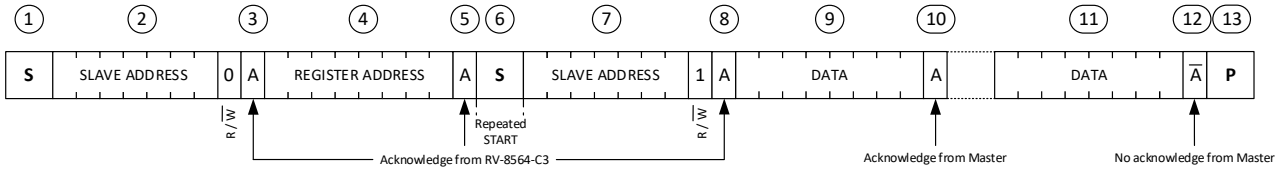
1) Master sends out the START condition.
2) Master sends out Slave Address, A2h for the RV-8564-C3; the R/$\overline{W}$ bit is a 0 indicating a write operation.
3) Acknowledgement from RV-8564-C3.
4) Master sends out the Register Address to RV-8564-C3.
5) Acknowledgement from RV-8564-C3.
6) Master sends out the Data to write to the specified address in step 4).
7) Acknowledgement from RV-8564-C3.
8) Steps 6) and 7) can be repeated if necessary.
   The address is automatically incremented in the RV-8564-C3.
9) Master sends out the STOP Condition.



## 5.8. READ OPERATION AT SPECIFIC ADDRESS

Master reads data from slave RV-8564-C3 at specific address:

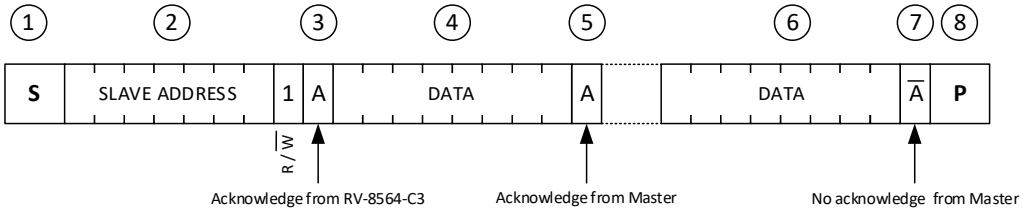
1) Master sends out the START condition.
2) Master sends out Slave Address, A2h for the RV-8564-C3; the R/$\overline{W}$ bit is a 0 indicating a write operation.
3) Acknowledgement from RV-8564-C3.
4) Master sends out the Register Address to RV-8564-C3.
5) Acknowledgement from RV-8564-C3.
6) Master sends out the Repeated START condition (or STOP condition followed by START condition).
7) Master sends out Slave Address, A3h for the RV-8564-C3; the R/$\overline{W}$ bit is a 1 indicating a read operation.
8) Acknowledgement from RV-8564-C3.
   At this point, the Master becomes a Receiver and the Slave becomes the Transmitter.
9) The Slave sends out the Data from the Register Address specified in step 4).
10) Acknowledgement from Master.
11) Steps 9) and 10) can be repeated if necessary.
    The address is automatically incremented in the RV-8564-C3.
12) The Master, addressed as Receiver, can stop data transmission by not generating acknowledge on the last byte that has been sent from the Slave-Transmitter. In this event, the Slave-Transmitter must leave the data line HIGH to enable the Master to generate a STOP condition.
13) Master sends out the STOP condition.




## 5.9. READ OPERATION

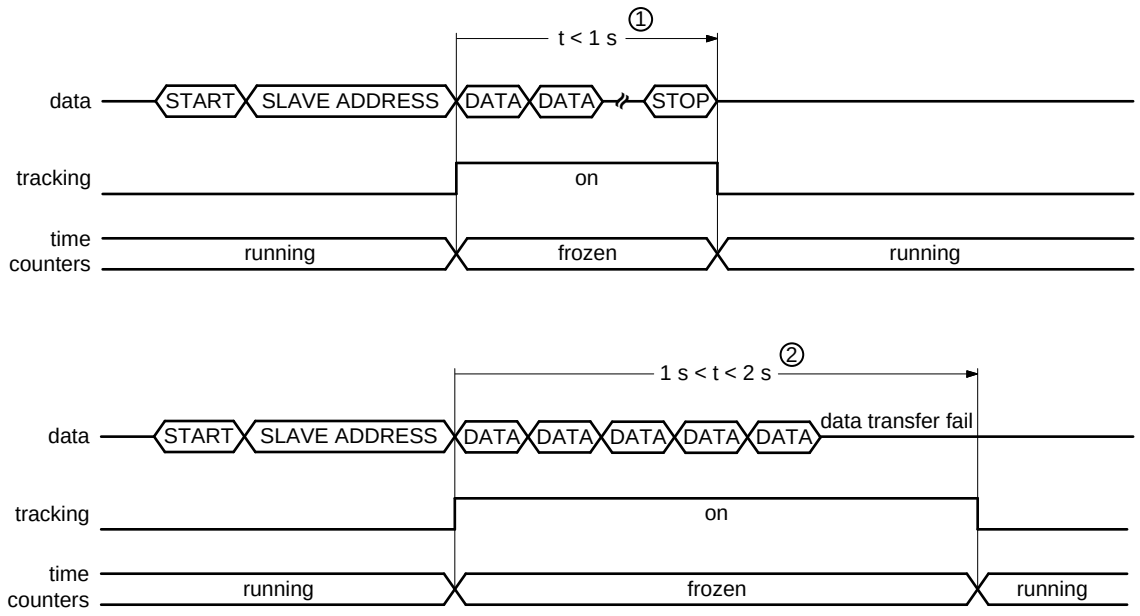
Master reads data from slave RV-8564-C3 immediately after first byte:

1) Master sends out the START condition.
2) Master sends out Slave Address, A3h for the RV-8564-C3; the R/$\overline{W}$ bit is a 1 indicating a read operation.
3) Acknowledgement from RV-8564-C3.
   At this point, the Master becomes a Receiver and the Slave becomes the Transmitter.
4) The RV-8564-C3 sends out the Data from the last accessed Register Address incremented by 1.
5) Acknowledgement from Master.
6) Steps 4) and 5) can be repeated if necessary.
   The address is automatically incremented in the RV-8564-C3.
7) The Master, addressed as Receiver, can stop data transmission by not generating acknowledge on the last byte that has been sent from the Slave-Transmitter. In this event, the Slave-Transmitter must leave the data line HIGH to enable the Master to generate a STOP condition.
8) Master sends out the STOP condition.



## 5.10. FREEZE AND BUS TIMEOUT FUNCTION

Correct and incorrect data transfer:




① Correct data transfer: read or write.
② Incorrect data transfer: read or write

During read/write operations, the time counting circuits are frozen. To prevent a situation where the currently accessed RTC module becomes locked and does not clear (unblock) the interface, the RV-8564-C3 has a built in bus timeout function. Should the interface be active for more than 1 s from the time a valid slave address is transmitted, then the RV-8564-C3 will automatically clear the interface and allow the time counting circuits to continue counting. The timeout function will trigger between 1 s and 2 s after receiving a valid slave address. Each time the timeout period is exceeded, 1 s will be lost from the time counters.
The bus timeout function is implemented to prevent the excessive loss of time due to interface access failure e.g. if main power is removed from a battery backed-up system during an interface access.

# 6. ELECTRICAL SPECIFICATIONS

## 6.1. ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings according to IEC 60134:

| SYMBOL | PARAMETER | CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{DD}$ | Power supply voltage | | -0.5 | 6.5 | V |
| $V_I$ | Input voltage | | -0.5 | 6.5 | V |
| $V_O$ | Output voltage | | -0.5 | 6.5 | V |
| $P_{TOT}$ | Total power dissipation | | | 300 | mW |
| $V_{ESD}$ | Electrostatic discharge Voltage | HBM (1) | | ±3500 | V |
| $I_{LU}$ | Latch-up current | (2) | | ±100 | mA |
| $T_{OPR}$ | Operating temperature range | | -40 | 85 | °C |
| $T_{STO}$ | Storage temperature | Stored as bare product | -55 | 125 | °C |
| $T_{PEAK}$ | Maximum reflow condition | JEDEC J-STD-020C | | 265 | °C |

(1) HBM: Human Body Model, according to JESD22-A114.
(2) Latch-up testing, according to JESD78 at maximum operating temperature ($T_{OPR(MAX)}$ = +85°C).

## 6.2. OPERATING PARAMETERS

For this Table, $V_{DD}$ = 1.2 to 5.5 V; $V_{SS}$ = 0V; $T_A$ = -40 °C to +85 °C; TYP values at 25 °C and 3.0 V; unless otherwise indicated.

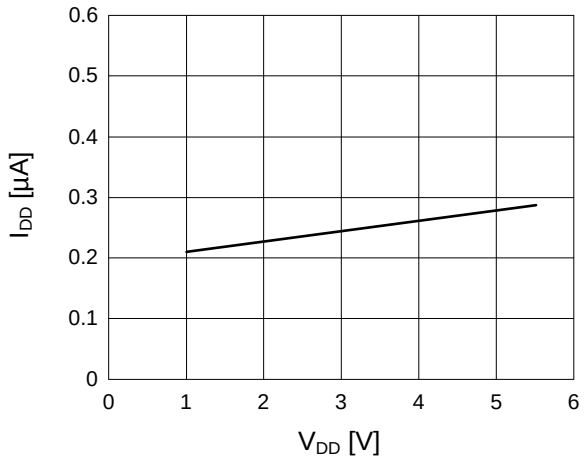
Operating Parameters:

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Supply** | | | | | | |
| $V_{DD}$ | Power supply voltage | Time-keeping mode; interface inactive; $f_{SCL}$ = 0 Hz | 1.2 | | 5.5 | V |
| | | Interface active; $f_{SCL}$ = 400 kHz | 1.8 | | 5.5 | |
| | | For clock data integrity; $T_A$ = 25 °C | $V_{LOW}$ | | 5.5 | |
| $I_{DD}$ | $V_{DD}$ supply current. Interface active | $f_{SCL}$ = 400 kHz | | | 800 | µA |
| | | $f_{SCL}$ = 100 kHz | | | 200 | |
| $I_{DD}$ | $V_{DD}$ supply current timekeeping. Interface inactive ($f_{SCL}$ = 0 Hz); CLKOUT disabled; $T_A$ = 25°C (1) (2) (3) | $V_{DD}$ = 5.0 V | | 275 | 550 | nA |
| | | $V_{DD}$ = 3.0 V | | 250 | 500 | |
| | | $V_{DD}$ = 2.0 V | | 225 | 450 | |
| $I_{DD}$ | $V_{DD}$ supply current timekeeping. Interface inactive ($f_{SCL}$ = 0 Hz); CLKOUT disabled; $T_A$ = -40 to +85°C (1) (2) (3) | $V_{DD}$ = 5.0 V | | 500 | 750 | nA |
| | | $V_{DD}$ = 3.0 V | | 400 | 650 | |
| | | $V_{DD}$ = 2.0 V | | 400 | 600 | |
| $I_{DD}$ | $V_{DD}$ supply current. Interface inactive ($f_{SCL}$ = 0 Hz); CLKOUT enabled (32.768 kHz); no load; $T_A$ = 25°C (3) (4) (5) | $V_{DD}$ = 5.0 V | | 1.5 | 3.0 | µA |
| | | $V_{DD}$ = 3.0 V | | 1.0 | 2.0 | |
| | | $V_{DD}$ = 2.0 V | | 0.7 | 1.4 | |
| $I_{DD}$ | $V_{DD}$ supply current (example). Interface inactive ($f_{SCL}$ = 0 Hz); CLKOUT enabled (32.768 kHz); $C_L$ = 7.5 pF; $T_A$ = 25°C (3) | $V_{DD}$ = 5.0 V | | 2.5 | 3.4 | µA |
| | | $V_{DD}$ = 3.0 V | | 1.5 | 2.2 | |
| | | $V_{DD}$ = 2.0 V | | 1.1 | 1.6 | |
| **Inputs** | | | | | | |
| $V_I$ | Input voltage | On pins SDA and SCL | -0.5 | | 5.5 | V |
| | | On pin CLKOE | -0.5 | | $V_{DD}$ +0.5 | |
| $V_{IL}$ | LOW level input voltage | | | | 0.3 $V_{DD}$ | V |
| $V_{IH}$ | HIGH level input voltage | | 0.7 $V_{DD}$ | | | V |
| $I_{LI}$ | Input leakage current | $V_I$ = $V_{SS}$ or $V_{DD}$ | | 0 | | µA |
| | | $V_I$ = $V_{SS}$ or $V_{DD}$, post ESD event | -1 | | +1 | µA |
| $C_I$ | Input capacitance (6) | | | | 7 | pF |
| **Outputs** | | | | | | |
| $V_O$ | Output voltage | On pin CLKOUT | -0.5 | | $V_{DD}$ +0.5 | V |
| | | On pin $\overline{INT}$ | -0.5 | | 5.5 | |
| $I_{OH}$ | HIGH level output current | Output source current | | | | |
| | | On pin CLKOUT $V_{OH}$ = 4.6 V, $V_{DD}$ = 5.0 V | 1 | | | mA |
| $I_{OL}$ | LOW level output current | Output sink current | | | | |
| | | On pin SDA $V_{OL}$ = 0.4 V, $V_{DD}$ = 5.0 V | 3 | | | mA |
| | | On pin $\overline{INT}$ $V_{OL}$ = 0.4 V, $V_{DD}$ = 5.0 V | 1 | | | mA |
| | | On pin CLKOUT $V_{OL}$ = 0.4 V, $V_{DD}$ = 5.0 V | 1 | | | mA |
| $I_{LO}$ | Output leakage current | $V_O$ = $V_{SS}$ or $V_{DD}$ | | 0 | | µA |
| | | $V_O$ = $V_{SS}$ or $V_{DD}$, post ESD event | -1 | | +1 | µA |
| **Voltage detector** | | | | | | |
| $V_{LOW}$ | Low voltage | $T_A$ = 25 °C | | 0.9 | 1.0 | V |

(1) Timer Clock Frequency = 1/60 Hz.
(2) CLKOUT disabled (FE = 0 or CLKOE = 0).
(3) $V_{IL}$ and $V_{IH}$ with an input voltage swing of $V_{SS}$ to $V_{DD}$.
(4) CLKOUT is open circuit.
(5) Current consumption when the CLKOUT pin is enabled is a function of the load on the pin, the output frequency, and the supply voltage. The additional current consumption for a given load is calculated from: $\Delta I_{DD} = C_L \times V_{DD} \times F_{CLKOUT}$.
(6) Tested on sample basis.

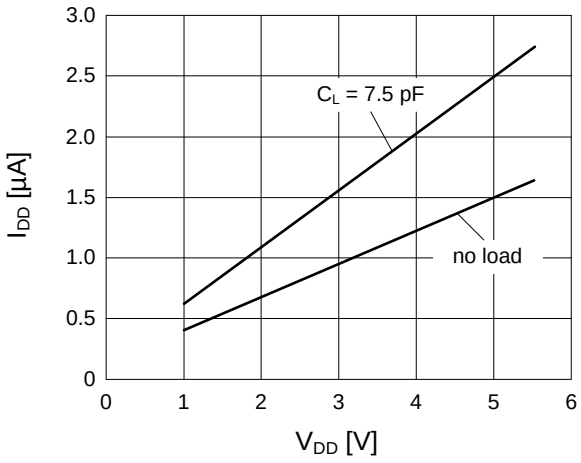
## 6.3. TYPICAL CHARACTERISTICS

$I_{DD}$ as a function of $V_{DD}$



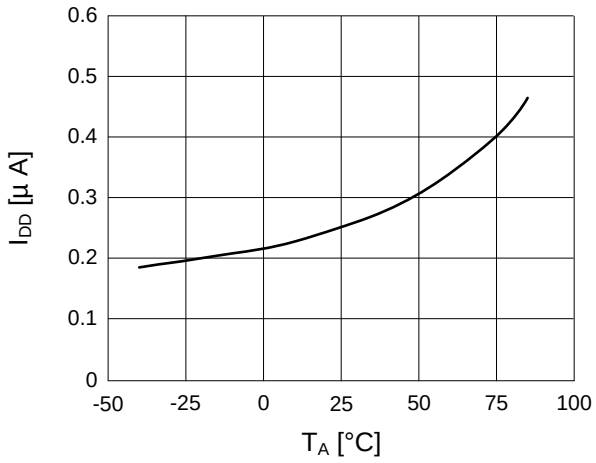

$T_A$ = 25°C; timer = 1/60 Hz; CLKOUT disabled.

$I_{DD}$ as a function of $V_{DD}$



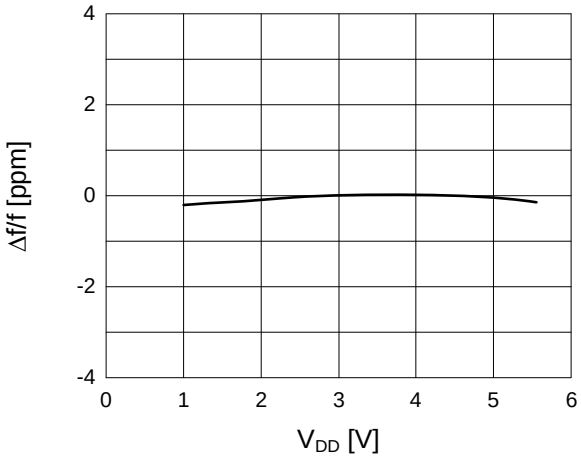

$T_A$ = 25°C; timer = 1/60 Hz; CLKOUT = 32.768 kHz.

$I_{DD}$ as a function of temperature




$V_{DD}$ = 3 V; timer = 1/60 Hz; CLKOUT disabled.

Frequency deviation as a function of $V_{DD}$




$T_A$ = 25°C; normalized to $V_{DD}$ = 3 V.

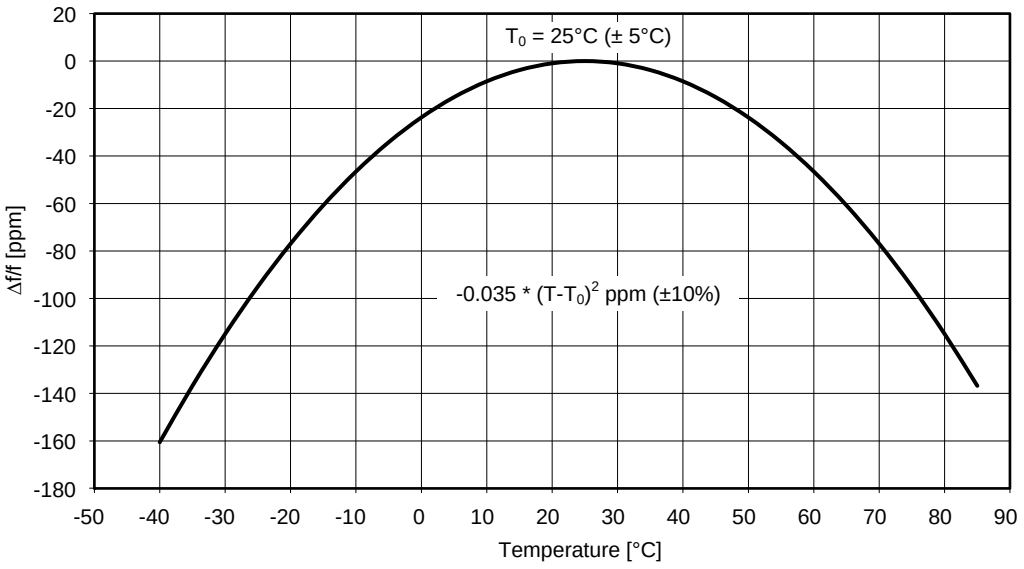
## 6.4. OSCILLATOR PARAMETERS

For this Table, $V_{DD}$ = 3.0 V; $V_{SS}$ = 0V; $T_A$ = 25 °C; unless otherwise indicated.

Oscillator Parameters:

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Xtal General** | | | | | | |
| f | Crystal Frequency | | | 32.768 | | kHz |
| $t_{START}$ | Oscillator start-up time | | | 0.35 | 0.5 | s |
| $\delta_{CLKOUT}$ | CLKOUT duty cycle | $F_{CLKOUT}$ = 32.768 kHz | 40 | | 60 | % |
| **Xtal Frequency Characteristics** | | | | | | |
| Δf/f | Frequency accuracy | | | ±10 | ±20 | ppm |
| Δf/V | Frequency vs. voltage characteristics | 1.8V ≤ $V_{DD}$ ≤ 5.5 V | | | ±1.5 | ppm/V |
| $\Delta f/f_{TOPR}$ | Frequency vs. temperature characteristics | $T_{OPR}$ = -40°C to +85°C<br>$V_{DD}$ = 3.0 V | $-0.035^{ppm}/_{°C^2}$ $(T_{OPR}-T_0)^2$ ±10% | | | ppm |
| $T_0$ | Turnover temperature | | 20 | | 30 | °C |
| Δf/f | Aging first year max. | | | | ±3 | ppm |

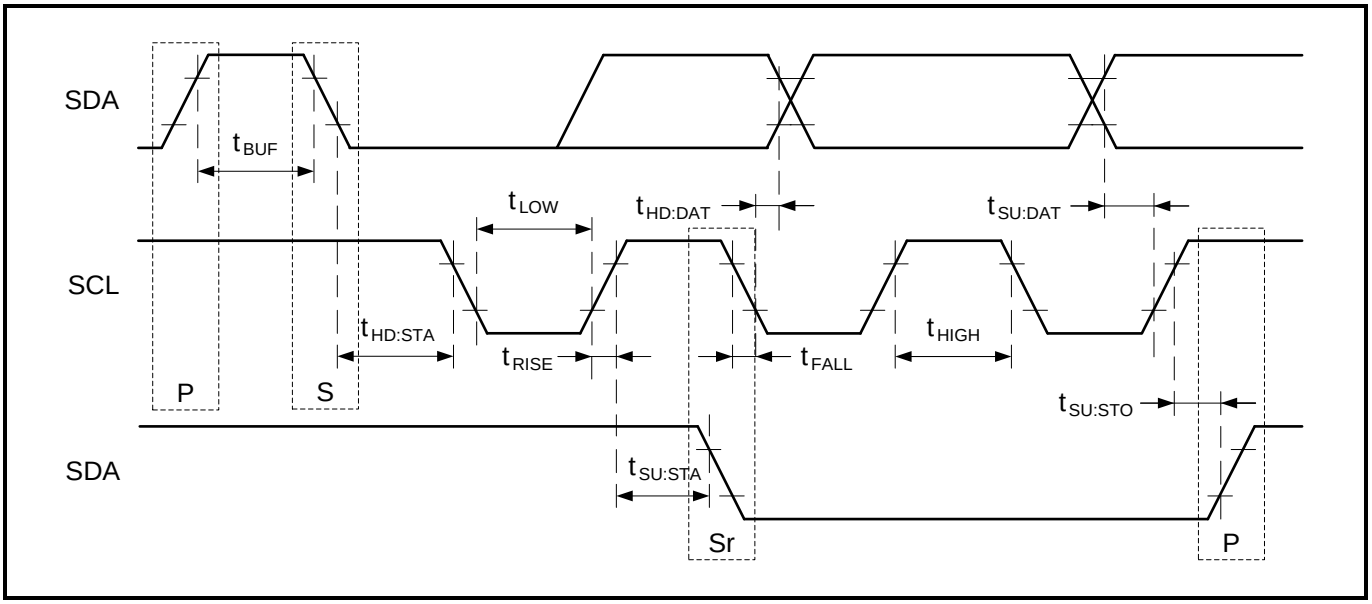
### 6.4.1.XTAL FREQUENCY VS. TEMPERATURE CHARACTERISTICS



## 6.5. I²C-BUS CHARACTERISTICS

The following Figure and Table describe the I²C-bus interface AC electrical parameters.

I²C-bus interface AC Parameter Definitions:




For the following Table, $V_{DD}$ = 1.8 to 5.5 V; $V_{SS}$ = 0V; $T_A$ = -40 °C to +85 °C.

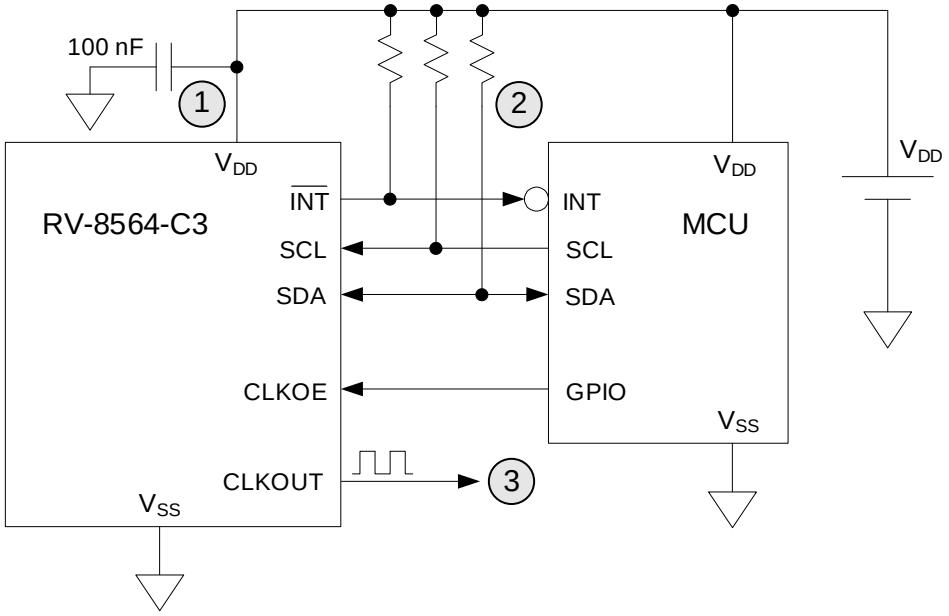
I²C-bus interface AC Electrical Parameters:

| SYMBOL | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $f_{SCL}$ | SCL input clock frequency | | | 400 | kHz |
| $t_{LOW}$ | Low period of SCL clock | 1.3 | | | µs |
| $t_{HIGH}$ | High period of SCL clock | 0.6 | | | µs |
| $t_{RISE}$ | Rise time of SDA and SCL | | | 300 | ns |
| $t_{FALL}$ | Fall time of SDA and SCL | | | 300 | ns |
| $C_b$ | Capacitive load for each bus line | | | 400 | pF |
| $t_{HD:STA}$ | START condition hold time | 0.6 | | | µs |
| $t_{SU:STA}$ | START condition setup time | 0.6 | | | µs |
| $t_{SU:DAT}$ | SDA setup time | 100 | | | ns |
| $t_{HD:DAT}$ | SDA hold time | 0 | | | µs |
| $t_{SU:STO}$ | STOP condition setup time | 0.6 | | | µs |
| $t_{BUF}$ | Bus free time before a new transmission | 1.3 | | | µs |
| $t_{SP}$ | Spike pulse width | | | 50 | ns |
| S = Start condition, Sr = Repeated Start condition, P = Stop condition | | | | | |

**Caution:**
When communicating with the RV-8564-C3 module, the series of operations from transmitting the START (or repeated START) condition to transmitting the STOP (or repeated START) condition should occur within 1 second. If this series of operations requires 1 second or more, the I²C-bus interface will be automatically cleared and set to standby mode by the bus timeout function of the RV-8564-C3 module.

# 7. TYPICAL APPLICATION CIRCUITS

## 7.1. OPERATING RV-8564-C3



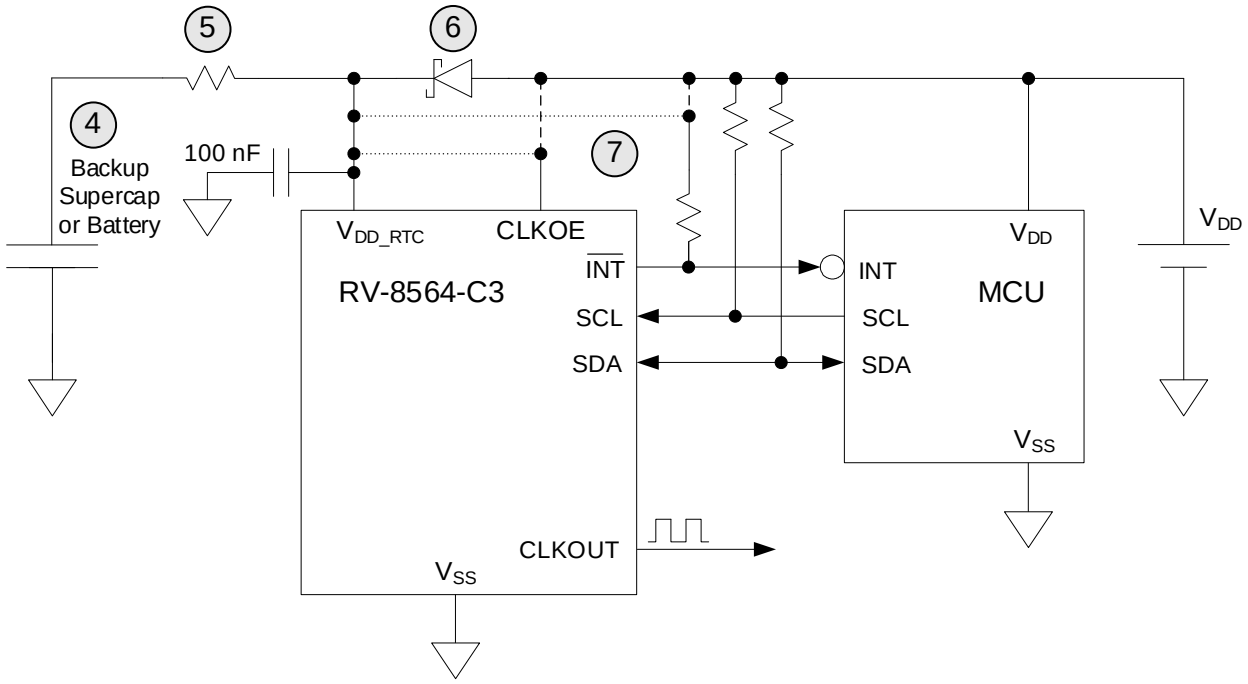

1. A 100 nF decoupling capacitor is recommended close to the device.

2. Interface lines SCL, SDA and the $\overline{INT}$ output are open drain and require pull-up resistors to $V_{DD}$.

3. CLKOUT offers selectable frequencies of 32.768 kHz (default), 1024 Hz, 32 Hz and 1 Hz for application use. If not used, it is recommended to disable CLKOUT for optimized current consumption by setting FE to 0 or by pulling CLKOE LOW. When disabled, the CLKOUT is LOW.
Further current minimization can be achieved by turning off the timer (TE = 0) and setting the timer clock frequency to 1/60 Hz (TD = 11b).

## 7.2. OPERATING RV-8564-C3 WITH BACKUP CAPACITOR

An external diode-circuitry can be wired to ensure standby or back-up supply. With the RTC in its minimum power configuration (see OPERATING RV-8564-C3) the RTC with a supercapacitor may operate for weeks and with a battery for years.




4 Supercapacitor (e.g. 1 farad), primary battery or secondary battery LMR (respect manufacturer specifications for constant charging voltage).

5 When using a supercapacitor, a resistor is used to limit the inrush current into the supercapacitor at power-on. E.g. to comply with the maximum forward current of the schottky diode.
or
When using a battery, a resistor is used to limit the maximum current in case of a short circuit.

6 Schottky diode. This low $V_F$ diode (less than 0.3 V) is needed to not exceed the specified maximum voltage at the inputs of the RV-8564-C3 when normal supply voltage $V_{DD}$ is present ($V_{I\_MAX} = V_{DD\_RTC}$ +0.5V). Schottky diodes have considerable leakage currents. To optimize backup time it is recommended to select a low leakage Schottky (e.g. BAS70-05).

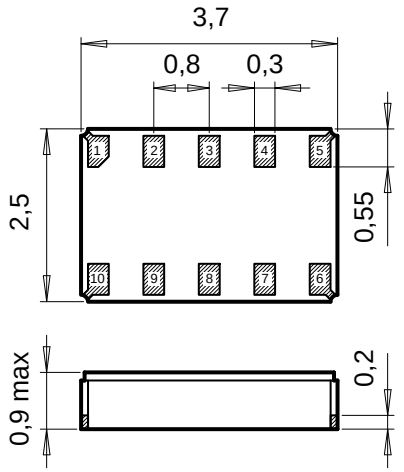
7 If the clock signal (pin CLKOUT) and/or the interrupt signal (pin $\overline{INT}$) are required in backup mode ($V_{DD\_RTC}$) the CLKOE pin and/or the pull-up resistor for the $\overline{INT}$ pin can be connected to $V_{DD\_RTC}$.

# 8. PACKAGE

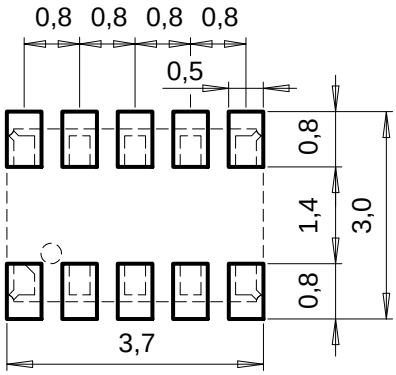
## 8.1. DIMENSIONS AND SOLDER PAD LAYOUT

**RV-8564-C3 Package:**

Package dimensions (bottom view):




Recommended solder pad layout:



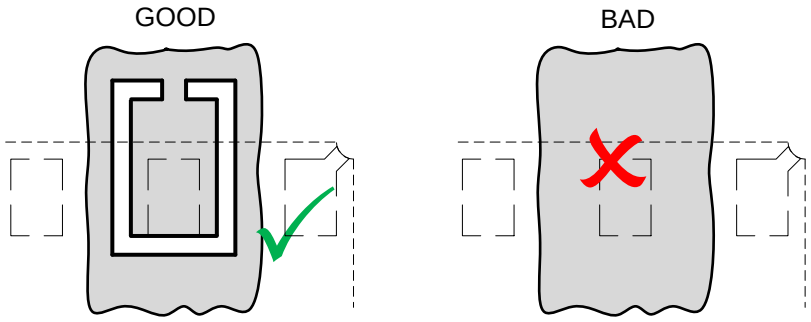

Metal lid is connected to $V_{SS}$ (pin #7)

| | |
|---|---|
| Dimensions: | in mm |
| Tolerances: | unless otherwise specified ±0.1 mm |
| Drawing: | RV-8564-C3_Pack-drw_20170511 |

### 8.1.1.RECOMMENDED THERMAL RELIEF

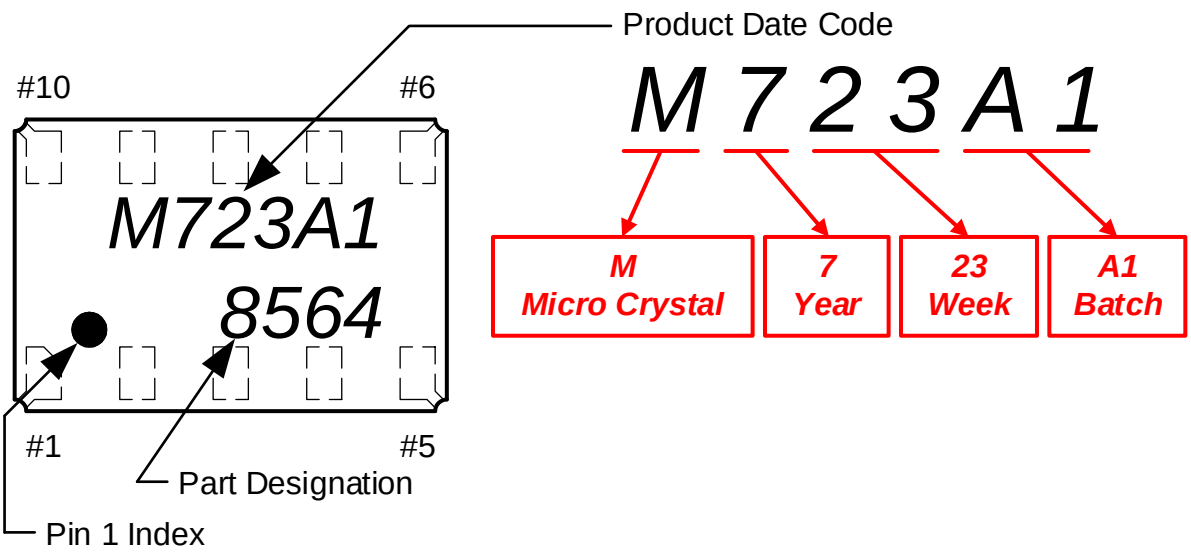
When connecting a pad to a copper plane, thermal relief is recommended.

**RV-C3 Package:**



## 8.2. MARKINGS AND PIN #1 INDEX

**Laser marking RV-8564-C3 Package: (top view)**

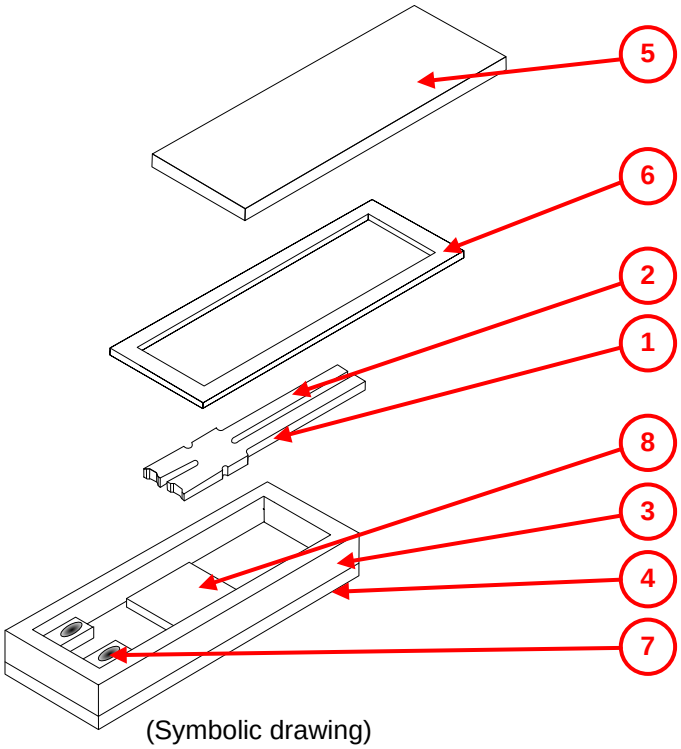


# 9. MATERIAL COMPOSITION DECLARATION & ENVIRONMENTAL INFORMATION

## 9.1. HOMOGENOUS MATERIAL COMPOSITION DECLARATION RV-8564-C3

Homogenous material information according to IPC-1752 standard

**Material Composition RV-8564-C3:**




(Symbolic drawing)

| No. | Item Component Name | Sub Item Material Name | Material Weight (mg) | (%) | Substance Element | CAS Number | Comment |
|---|---|---|---|---|---|---|---|
| **1** | Resonator | Quartz Crystal | 0.32 | 100% | $SiO_2$ | 14808-60-7 | |
| **2** | Electrodes | Cr+Au | 0.01 | 6% | Cr | Cr: 7440-47-3 | |
| | | | | 94% | Au | Au: 7440-57-5 | |
| **3** | Housing | Ceramic | 15.65 | 100% | $Al_2O_3$ | 1344-28-1 | |
| **4** | Terminations | Internal and extrenal terminals | 0.38 | 80% | W | W: 7440-33-7 | Tungsten |
| | | | | 15% | Ni | Ni: 7440-02-0 | Nickel plating |
| | | | | 5% | Au 0.5 micron | Au: 7440-57-5 | Gold plating |
| **5** | Metal Lid | Kovar Lid | 6.91 | 95% | Fe53Ni29Co18 | Fe: 7439-89-6<br>Ni: 7440-02-0<br>Co: 7440-48-4 | Metal Lid (Kovar) |
| | | Ni-plating | | 4.95% | Ni | Ni: 7440-02-0 | Nickel plating |
| | | Au-plating | | 0.05% | Au | Au: 7440-57-5 | Gold plating |
| **6** | Seal | Solder Preform | 1.00 | 80% | Au80 / Sn20 | Au: 7440-57-5 | Premelted on Metal Lid |
| | | | | 20% | | Sn: 7440-31-5 | |
| **7** | Conductive adhesive | Silver filled Silicone glue | 0.09 | 88% | Ag | Ag: 7440-22-4 | |
| | | | | 12% | Siloxanes and silicones | 68083-19-2 | di-Me, vinyl group-terminated |
| | | | | 0% | Distillates, petroleum hydrotreated | 64742-47-8 | Does not appear in finished product |
| **8** | CMOS IC | Silicon | 0.64 | 80% | Si | Si: 7440-21-3 | |
| | | Gold bumps | | 20% | Au | Au: 7440-57-5 | |
| | | Unit weight | 25.0 | | | | |

## 9.2. MATERIAL ANALYSIS & TEST RESULTS RV-8564-C3

Homogenous material information according to IPC-1752 standard

| No. | Item Component Name | Sub Item Material Name | RoHS | | | | | | Halogens | | | | Phthalates | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Pb | Cd | Hg | Cr(VI) | PBB | PBDE | F | Cl | Br | I | BBP | DBP | DEHP | DINP |
| **1** | Resonator | Quartz Crystal | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd |
| **2** | Electrodes | Cr+Au | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd |
| **3** | Housing | Ceramic | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd |
| **4** | Terminations | Int. & ext. terminals | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd |
| **5** | Metal Lid | Kovar Lid & Plating | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd |
| **6** | Seal | Solder Preform | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd |
| **7** | Conductive adhesive | Silver filled Silicone glue | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd |
| **8** | CMOS IC | Silicon & Gold bumps | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd |
| | MDL [ppm] | Method Detection Limit | 2 | | | 8 | 5 | | 50 | | | | 50 | | | |

nd (not detected) = below “Method Detection Limit” (MDL)

**Test methods:**

**RoHS** Test method with reference to:

- Pb, Cd IEC 62321-5:2013 MDL: 2 ppm
- Hg IEC 62321-4:2013 + AMD1:2017 MDL: 2 ppm
- Cr(VI) IEC 62321-7-2:2017 MDL: 8 ppm
- PBB / PBDE IEC 62321-6:2015 MDL: 5 ppm

**Halogens** Test method with reference to BS EN 14582:2016 MDL: 50 ppm

**Phthalates** Test method with reference to IEC 62321-8:2017 MDL: 50 ppm

## 9.3. RECYCLING MATERIAL INFORMATION RV-8564-C3

Recycling material information according to IPC-1752 standard.
Element weight is accumulated and referenced to the unit weight of 25.0 mg.

| Item Material Name | No. | Item Component Name | Material Weight (mg) | Material Weight (%) | Substance Element | CAS Number | Comment |
|---|---|---|---|---|---|---|---|
| Quartz Crystal | 1 | Resonator | 0.32 | 1.28 | $SiO_2$ | 14808-60-7 | |
| Chromium | 2 | Electrodes | 0.0006 | 0.002 | Cr | Cr: 7440-47-3 | |
| Ceramic | 3 | Housing | 15.65 | 62.60 | $Al_2O_3$ | 1344-28-1 | |
| Gold | 2<br>4<br>5<br>6<br>8 | Electrodes<br>Terminations<br>Metal Lid<br>Seal<br>CMOS IC | 0.96 | 3.84 | Au | Au: 7440-57-5 | |
| Tungsten | 4 | Terminations | 0.30 | 1.22 | W | W: 7440-33-7 | |
| Nickel | 4<br>6 | Terminations<br>Metal Lid | 0.40 | 1.60 | Ni | Ni: 7440-02-0 | |
| Kovar | 5 | Metal Lid | 6.56 | 26.26 | Fe53Ni29Co18 | Fe: 7439-89-6<br>Ni: 7440-02-0<br>Co: 7440-48-4 | |
| Tin | 6 | Seal | 0.20 | 0.80 | Sn | Sn: 7440-31-5 | |
| Silver | 7a | Conductive adhesive | 0.079 | 0.32 | Ag | Ag: 7440-22-4 | |
| Siloxanes and silicones | 7b | Conductive adhesive | 0.011 | 0.04 | Siloxanes and silicones | 68083-19-2 | di-Me, vinyl group-terminated |
| Distillates | 7c | Conductive adhesive | 0 | 0 | Distillates | 64742-47-8 | hydrotreated petroleum, does not appear in finished products |
| Silicon | 8 | CMOS IC | 0.51 | 2.05 | Si | Si: 7440-21-3 | |
| | Unit weight (total) | | 25.0 | 100 | | | |

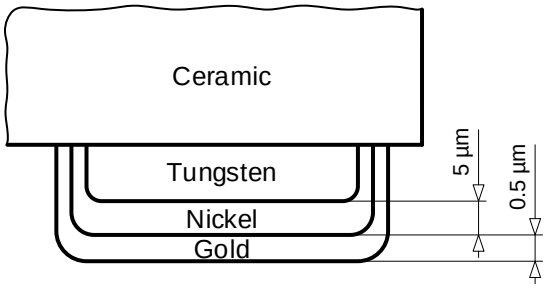
## 9.4. ENVIRONMENTAL PROPERTIES & ABSOLUTE MAXIMUM RATINGS RV-8564-C3

| Package | Description |
|---|---|
| SON-10 ceramic package | Small Outline Non-leaded (SON), hermetically sealed ceramic package with metal lid. |

| Parameter | Directive | Conditions | Value |
|---|---|---|---|
| Shelf life | | Warehouse conditions * | minimum 5 years |
| Product weight (total) | | | 25.0 mg |
| Storage temperature | | Store as bare product | -55 to +125°C |
| Moisture sensitivity level (MSL) | IPC/JEDEC J-STD-020D | | MSL1 |
| FIT / MTBF | | | available on request |

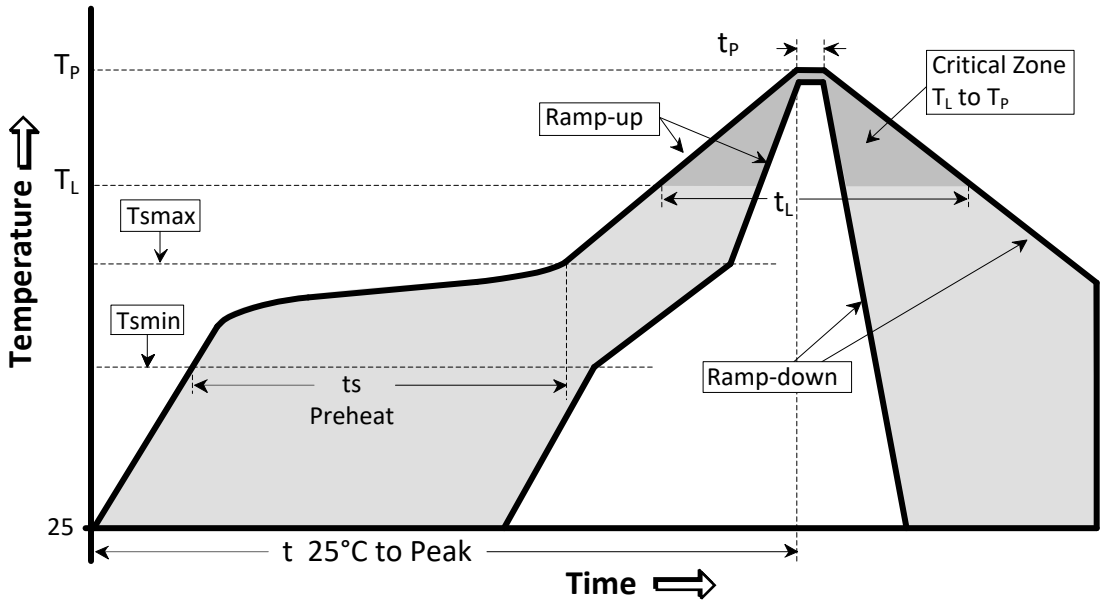
* From the date code on the product, sealed in the original packaging.

Terminal finish:



## 9.5. SOLDERING INFORMATION

**Maximum Reflow Conditions in accordance with IPC/JEDEC J-STD-020C "Pb-free"**




| Temperature Profile | Symbol | Condition | Unit |
|---|---|---|---|
| Average ramp-up rate | ($Ts_{max}$ to $T_P$) | 3°C / second max | °C / s |
| Ramp down Rate | $T_{cool}$ | 6°C / second max | °C / s |
| Time 25°C to Peak Temperature | $T_{to\text{-}peak}$ | 8 minutes max | min |
| **Preheat** | | | |
| Temperature min | $Ts_{min}$ | 150 | °C |
| Temperature max | $Ts_{max}$ | 200 | °C |
| Time $Ts_{min}$ to $Ts_{max}$ | ts | 60 – 180 | sec |
| **Soldering above liquidus** | | | |
| Temperature liquidus | $T_L$ | 217 | °C |
| Time above liquidus | $t_L$ | 60 – 150 | sec |
| **Peak temperature** | | | |
| Peak Temperature | Tp | 260 | °C |
| Time within 5°C of peak temperature | tp | 20 – 40 | sec |

## 9.6. HANDLING PRECAUTIONS FOR MODULES WITH EMBEDDED CRYSTALS

The built-in tuning-fork crystal consists of pure Silicon Dioxide in crystalline form. The cavity inside the package is evacuated and hermetically sealed in order for the crystal blank to function undisturbed from air molecules, humidity and other influences.

**Shock and vibration:**

Keep the crystal / module from being exposed to **excessive mechanical shock and vibration**. Micro Crystal guarantees that the crystal / module will bear a mechanical shock of 5000 g / 0.3 ms.

The following special situations may generate either shock or vibration:

**Multiple PCB panels -** Usually at the end of the pick & place process the single PCBs are cut out with a router. These machines sometimes generate vibrations on the PCB that have a fundamental or harmonic frequency close to 32.768 kHz. This might cause breakage of crystal blanks due to resonance. Router speed should be adjusted to avoid resonant vibration.

**Ultrasonic cleaning -** Avoid cleaning processes using ultrasonic energy. These processes can damage the crystals due to the mechanical resonance frequencies of the crystal blank.

**Overheating, rework high temperature exposure:**

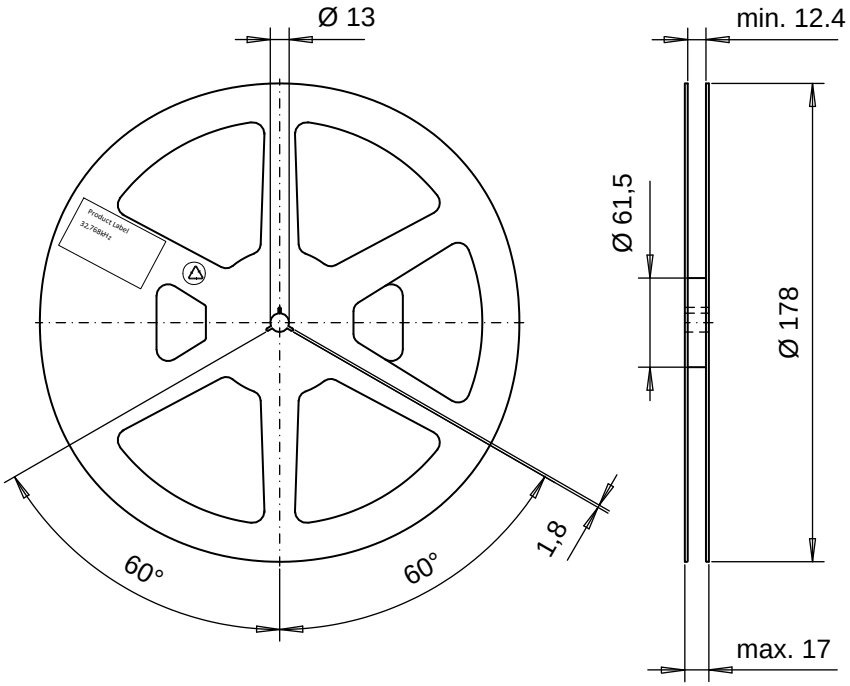
Avoid overheating the package. The package is sealed with a seal ring consisting of 80% Gold and 20% Tin. The eutectic melting temperature of this alloy is at 280°C. Heating the seal ring up to >280°C will cause melting of the metal seal which then, due to the vacuum, is sucked into the cavity forming an air duct. This happens when using hot-air-gun set at temperatures >280°C.

Use the following methods for rework:

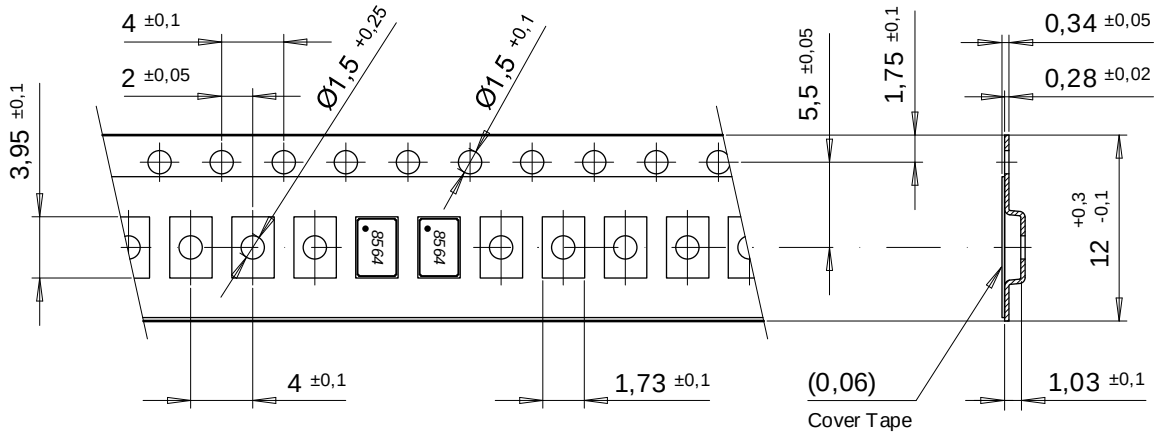
- Use a hot-air-gun set at 270°C.
- Use 2 temperature controlled soldering irons, set at 270°C, with special-tips to contact all solder-joints from both sides of the package at the same time, remove part with tweezers when pad solder is liquid.

## 10. PACKING & SHIPPING INFORMATION RV-8564-C3

**Reel:** 7” = 178 mm




**Carrier Tape:**
Material: Polycarbonate, conductive
Width: 12 mm
Tape Leader and Trailer: Minimum length 300 mm




**Pressure Seal Cover Tape:**
Polypropylene (PP)
3M™ Universal Cover Tape (UCT)
Synthetic polymer adhesive, pressure sensitive

Peel Method: Medial section removal,
both lateral stripes remain on carrier

**Heat Seal Cover Tape:**
Polyethylene Terephthalate (PET)
Synthetic polymer adhesive, heat activated

Peel Method: Removal of the entire cover tape

## 11. COMPLIANCE INFORMATION

Micro Crystal confirms that the standard product Real-Time Clock Module RV-8564-C3 is compliant with “EU RoHS Directive” and “EU REACh Directives”.
Please find the actual Certificate of Conformance for Environmental Regulations on our website:
CoC_Environment_RV-Series.pdf

## 12. DOCUMENT REVISION HISTORY

| Date | Revision # | Revision Details |
|---|---|---|
| February 2005 | 1.1 | First release |
| September 2005 | 1.2 | Add ESD protection schematic |
| July 2012 | 2.0 | Add C3 package version |
| October 2017 | 2.1 | Added various function descriptions and technical information<br>Added material composition declaration & environmental information |
| May 2025 | 2.2 | Created independent document version for RV-8564-C3 (old: RV-8564-Cx)<br>Added pin numbers to the Block Diagram, 2.<br>Added “Metal lid is connected to $V_{SS}$ (pin #7)”, 8.1.<br>Updated Marking and Pin #1 Index, 8.2.<br>Corrected numbering in the material composition drawing, 9.1.<br>Adapted limit values and methods in accordance with the latest standards, 9.2.<br>Completed to "hermetically sealed ceramic package with metal lid", 9.4.<br>Added shelf life, 9.4.<br>Corrected text to "hot-air-gun set at temperatures >280°C.", 9.6.<br>Adapted Cover/Carrier Tape height (0,06/0,34), 10.<br>Added specification for Heat Seal Cover Tape, 10.<br>Updated CoC Hyperlink, 11.<br>Added new disclaimer, 12. |



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