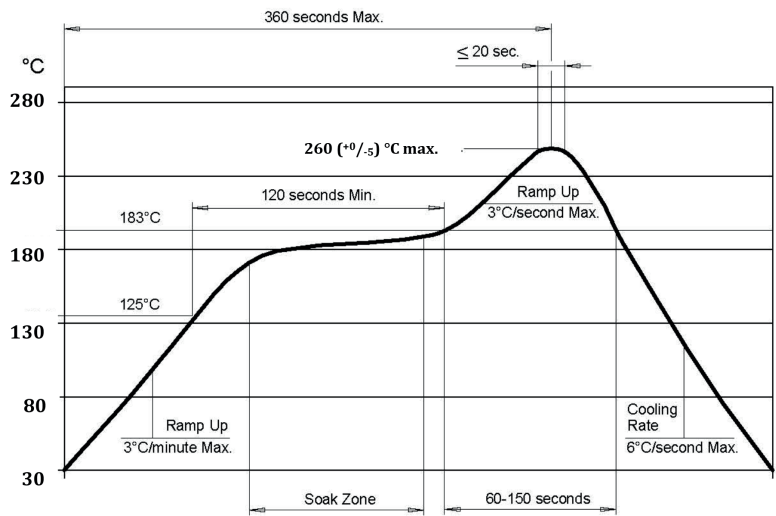# 1) Maximum Reflow Condition

Maximum Reflow Condition in accordance with JEDEC STD-020C.

Please note:
Using Infrared-Radiation for reflow-soldering results in unpredictable temperatures on the components. Parts could be over-heated and permanently damaged.
It is recommended not using IR-radiation for reflow-soldering.

2) Recommendations for Handling of Crystals oscillators in Ceramic Packages

Introduction

A crystal, compared to other passive elements, is a relatively fragile part due to its internal construction. The crystal blank consists of pure Silicon Dioxide in crystalline form, cut as small plate with a thickness of approximately 0.1 mm. The material is very similar to glass. The blank itself is attached at one end with 2 small dots of conductive epoxy on two small pedestals. The cavity inside the package is evacuated and hermetically sealed in order for the crystal blank to function undisturbed from air molecules, humidity and other influences.
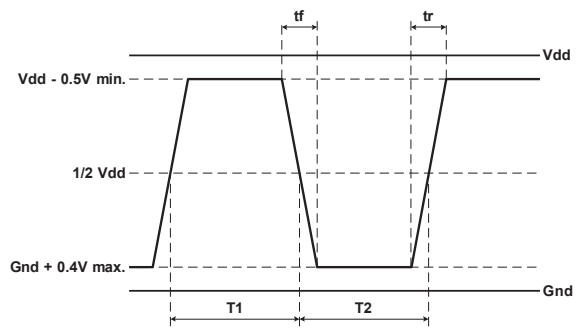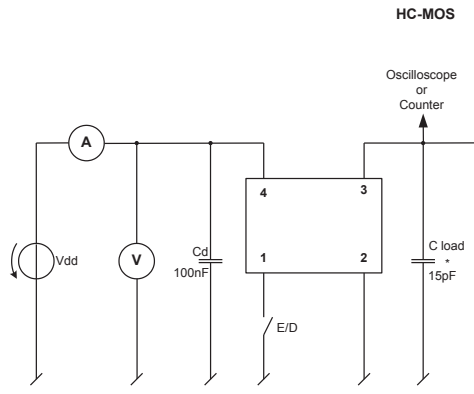
Precautions

- Shock and vibration - Keep the crystal from being exposed to **excessive mechanical shock and vibration** otherwise the crystal blank tends to break as any other glass would do. Micro Crystal guarantees that the crystal will bear a mechanical shock of 5000g / 0.3ms. The following special situations may generate either shock or vibration:

  → **Assembly machine selection** - During pick & place fast placing machines will generate shocks or vibrations when placing small elements. It is best to place the crystal on the second populated side of a two-sided PCB as the **last part,** preferably with a **slow placing machine** used to place complex or "odd form" parts.

- → **Multiple PCB panels** - Usually at the end of the pick & place process the single PCBs are cut out with a router. These machines sometimes generate vibrations on the PCB that have a fundamental or harmonic frequency close to 32.768 kHz. This might cause breakage of crystal blanks due to resonance. **Router speed should be adjusted** to avoid resonant vibration.

  → **Ultrasonic Washing and Welding** - Avoid washing or welding processes using **ultrasonic** energy. These processes can damages crystals due to mechanical resonance of the crystal blank.

  Thermal shocks - Avoid **steep temperature gradients.** It might lead to breakage of the crystal blank like it would do to any other glass. Infrared reflow processes in general are safe.

  Rework high temperature exposure - Avoid **overheating** the package. The package is sealed with a sealring consisting of 80% Gold and 20% Tin. The eutectic of this alloy is at 280°C. Heating the sealring up to 280°C will cause melting of the metal seal which then, due to the vacuum, is sucked into the cavity forming an air duct. Air molecules will impede (or slow) the movement of the tines causing the frequency to drop and the resistance to rise. In addition liquid metal might attach to the crystal blank further altering the parameters or causing a short circuit. Most of the time parts are overheated when removed from the PCB due to problems. If parts are removed (i.e. for analysis of failure mode) with excessive heat, all traces for root cause analysis will be lost. Therefore use the following methods for removal:

→ Use a hot **air gun** set at 260°C

→ Use **2 temperature controlled soldering irons,** set at 250°C, from both sides of the package at the same time, remove part with tweezers when pad solder is liquid.

3) Package description

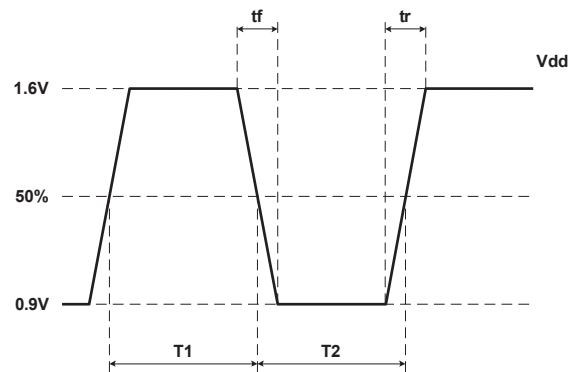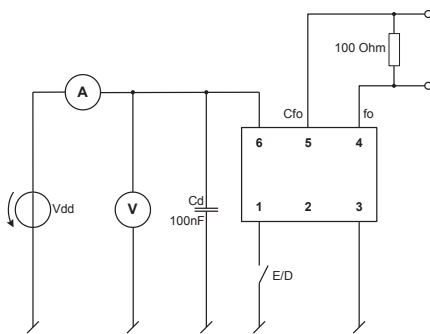| Package Description	
Package material	Ceramic Al2O3, black
Lid material	Ceramic Al2O3, black
Seal	Solder seal ring (preform)
Seal material	Au80/Sn20
Terminal	Gold (> 0.5 µm) over Ni (3 µm) over Tungsten
Moisture Sensitivity Level (MSL)	
Moisture Sensitivity Level (MSL) IPC/JEDEC J-STD-020-C (released July 2004)	The part is qualified and compliant to (MSL) Level 1

4) Application and Test Circuit: HC-MOS   Waveshape

HC-MOS

Oscilloscope
or
Counter

A

Vdd

V

Cd
100nF

4   3

1   2

C load
*
15pF

E/D

⚠ No power on E/D
function (pin 1) before
Vdd is setting on

tf   tr

Vdd

Vdd - 0.5V min.

1/2 Vdd

Gnd + 0.4V max.

Gnd

T1   T2

4) Application and Test Circuit: LVDS   Waveshape

A

Vdd

V

Cd
100nF

100 Ohm

Cfo   fo

6   5   4

1   2   3

E/D

⚠ No power on E/D
function (pin 1) before
Vdd is setting on

tf   tr

Vdd

1.6V

50%

0.9V

T1   T2

5) Marking

Description
Frequency
● Date code Serial Nb